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ARTICLE

Polarity-Tunable Photocurrent through Band Alignment Engineering in a High-Speed WSe_2/$SnSe_2$ Diode with Large Negative Responsivity

Sayantan Ghosh, Abin Varghese, Himani Jawa, Yuefeng Yin, Nikhil V. Medhekar, and Saurabh Lodha*

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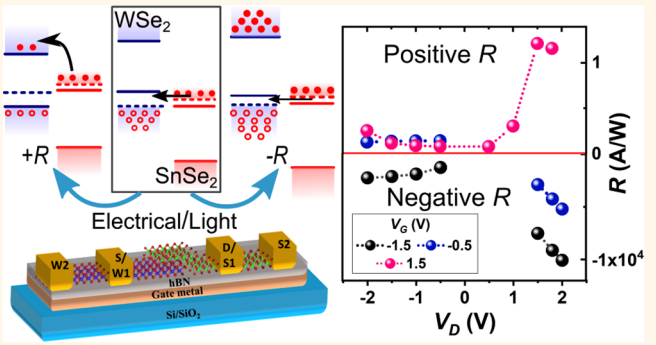
ABSTRACT: Excellent light−matter interaction and a wide range of thickness-tunable bandgaps in layered vdW materials coupled by the facile fabrication of heterostructures have enabled several avenues for optoelectronic applications. Realization of high photoresponsivity at fast switching speeds is a critical challenge for 2D optoelectronics to enable high-performance photodetection for optical communication. Moving away from conventional type-II heterostructure pn junctions towards a WSe_2/$SnSe_2$ type-III configuration, we leverage the steep change in tunneling current along with a light-induced heterointerface band shift to achieve high negative photoresponsivity, while the fast carrier transport under tunneling results in high speed. In addition, the photocurrent can be controllably switched from positive to negative values, with ~10^4× enhancement in responsivity, by engineering the band alignment from type-II to type-III using either the drain or the gate bias. This is further reinforced by electric-field dependent interlayer band structure calculations using density functional theory. The high negative responsivity of 2 × 10^4 A/W and fast response time of ~1 μs coupled with a polarity-tunable photocurrent can lead to the development of next-generation multifunctional optoelectronic devices.



KEYWORDS: *negative photocurrent, vdW heterostructure, type-III band alignment, tunnel conduction, photodetection*

INTRODUCTION

Layered two-dimensional (2D) transition metal dichalcogenides (TMDs) have gained immense importance in the area of photodetection due to their high light absorption coefficients[1] along with sizable and thickness-dependent electronic bandgaps.[2−4] Among the various photodetector architectures studied using 2D materials, pn heterojunctions of type-II nature have been well explored due to efficient separation of photocarriers, ease of fabrication, and possibility of broadband optical absorption.[5] Several such type-II heterojunctions with promising performance metrics have been reported in the literature, especially using group-VI TMDs, such as MoS_2, WS_2, WSe_2, $MoTe_2$, and ReS_2.[6−9] However, a bottleneck in 2D optoelectronics that needs to be addressed to fulfill its potential for technological applications is the realization of high photoresponsivity (R) along with ultrafast switching speed[10] to keep pace with rapid advancements in real time optical communication and image sensors-based technologies that are currently dominated by photodetectors relying on III−V materials, cadmium telluride, or Pb-based quantum dots.[11] Light incident on a photosensitive material typically results in an increase in charge carrier concentration through photogeneration resulting in the commonly observed positive photoconduction. However, the presence of traps, adsorbates, or interface engineering could enable the realization of negative photoconduction which has been exploited for low power and high-speed optoelectronics[12] and memory[13] as well as gas sensing applications.[14,15] The ability to controllably switch between positive and negative photoresponse in the same device, largely unrealized till now, could be desirable for photodetection with enhanced spectral resolution[16] as well as multilevel optical logic and memory.[13,16,17]

Recently, vdW tunnel field-effect transistors (FETs) have been studied for electronic applications due to their high

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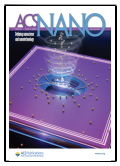

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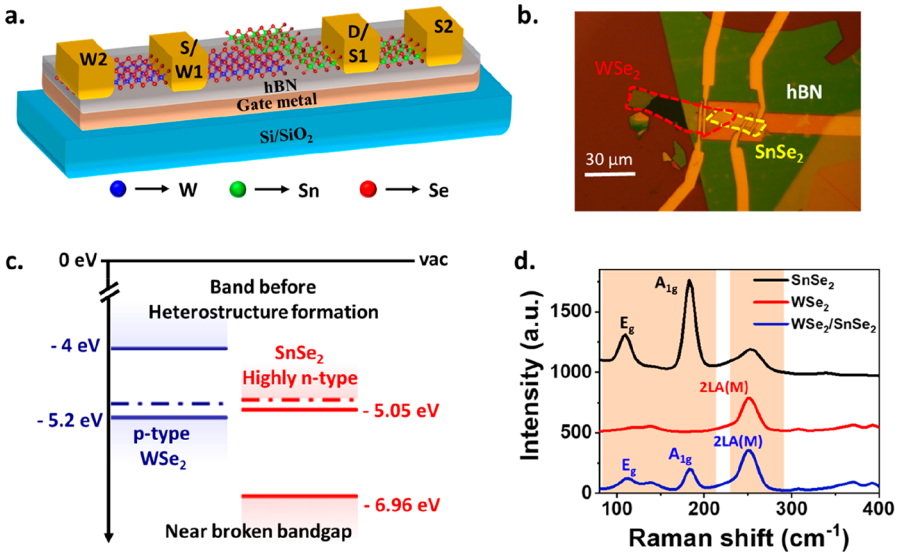

Figure 1. Device architecture, band alignment, and Raman spectra. (a) 3D schematic of the gated $WSe_2/SnSe_2$ heterojunction device. hBN is used as the bottom dielectric. (b) Optical microscope image of the device with top source/drain contacts on individual WSe_2 and $SnSe_2$ layers. The green layer on top of the bottom gate, which is patterned on a Si/SiO_2 substrate, corresponds to hBN. Red and yellow marked areas represent WSe_2 and $SnSe_2$ flakes, respectively. (c) Energy band diagrams of WSe_2 and $SnSe_2$ flakes before contact. (d) Raman spectra of individual WSe_2 and $SnSe_2$ flakes, as well as from the heterojunction region.

current density in the tunneling regime.[18,19] It has also been seen in conventional silicon-based tunnel diodes as well as in vdW heterostructures that, for band-to-band tunneling (BTBT), the subthreshold swing (SS) of a tunnel diode can beat the room temperature thermionic limit of 60 mV/dec.[20,21] This causes a sharper change in current with gate or drain[20] bias than in type-II junctions, where SS $\geq$ 60 mV/dec. Hence type-III tunnel photodiodes could be better-suited for simultaneous realization of high R and high speed due to two key attributes, (i) subthermionic regime of conduction that can favor a larger change in current upon illumination than type-II due to an optically induced change in interface band alignment (akin to a bias change) resulting in higher photocurrent (I_{ph}) and responsivity and (ii) the ability to turn the photocurrent on and off at high speed due to fast carrier transport under tunneling, which could result in shorter response times. Till now, a few studies in the field of 2D materials-based type-III photodetection have shown good photoresponse. Cao et al. have shown positive photoresponse with responsivity of 1×10^4 A/W in a type-III BP/ReS_2 system due to increased electron tunneling under illumination.[22] Here both BP and ReS_2 are highly doped p and n materials, respectively. In another study of $BP/SnSe_2$ type-III heterojunction Esaki diodes, positive photocurrent and a photoresponsivity of ~0.24 mA/W under zero bias applied has been reported.[23] Beyond operating the photodiode in type-III alignment wherein large and fast photoresponse can be realized, it can also be controllably switched to a conventional type-II alignment using gate/drain bias, which can enable tunable photoresponse that can be further exploited for multibit logic and memory applications. The $WSe_2/SnSe_2$ vdW stack forms a near-broken band alignment under equilibrium and is well studied electrically under type-III conduction as a tunnel diode as well as an FET.[21,24−26] However, such type-III heterodiodes demonstrating BTBT transport have been largely unexplored for optoelectronic applications, which is the major focus of the current study.

In this work, we demonstrate a gated few-layer $WSe_2/SnSe_2$ heterojunction photodiode which exhibits excellent photodetection metrics enabled by optically driven type-III band alignment engineering at the heterointerface and negative as well as positive photoresponse through a bias-driven type-III-to-type-II interface band line-up change. The electrical characteristics under dark indicate a change in transport mechanism from over the barrier (type-II) to tunneling (type-III) with drain and gate bias, which is reinforced through comprehensive electric-field dependent band structure calculations using density functional theory (DFT). Tunneling transport is further confirmed through temperature-dependent measurements of transfer characteristics of the $WSe_2/SnSe_2$ heterostructure in type-III configuration. Upon illumination with 532 nm light, steady state measurements show a large negative photocurrent under type-III band alignment, whereas type-II band alignment results in typically observed positive photocurrent. Temporal photocharacteristics reveal a fast response time (in microseconds) due to the ultrafast nature of carrier transport under BTBT[27] in contrast to the slow response times (in seconds) reported in trap or adsorbate-dependent negative photoresponse studies.[16,28,29] A maximum, ultrahigh negative R of 2×10^4 A/W with high speed switching comprising a response time of ~1 μs and a fall time of ~5 μs has been realized under the tunneling regime, making this one of the best high R−high speed vdW photodetectors, with the added capability of achieving voltage-driven tunable (negative as well as positive) photoresponse.

RESULTS

Photodetector Fabrication. A metal gate of 30 μm length and 20 μm width with an extended contact lead was fabricated on a SiO_2 (285 nm)/Si substrate using electron-beam (e-beam) lithography and metal sputtering. The gate was metallized using a Cr (2 nm)/Au (30 nm) stack. Next, an hBN flake was transferred selectively as a gate dielectric, such that it covered the entire metal gate area. Further, a thin WSe_2 flake was placed on top of the hBN flake such that the WSe_2

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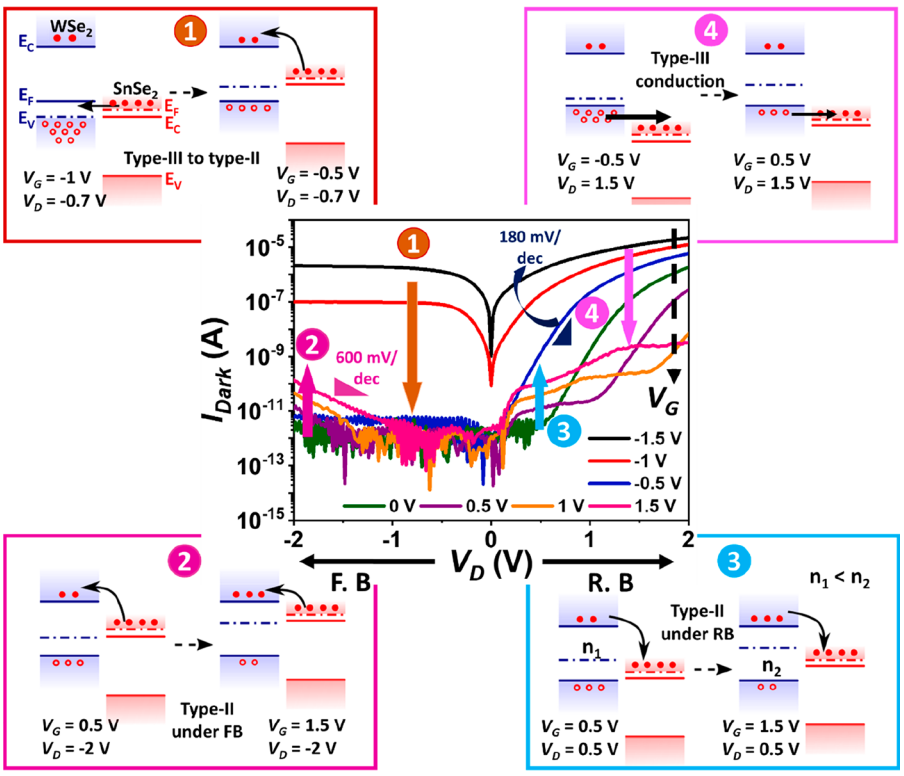

Figure 2. Device characterization under dark. Center plot represents gate tunable output characteristics of the $WSe_2/SnSe_2$ pn junction diode. The arrows 1 to 4 show transitions in the conduction mechanism under different V_G and V_D conditions, which are further elaborated through representative band diagrams in the four corner figure sections. Section 1 depicts the transition from type-III to type-II with change in V_G under FB. Section 2 explains the increasing drain current under type-II conduction with increasing positive V_G under high FB. Section 3 shows an increasing drain current with increasing positive V_G under RB. Lastly, section 4 demonstrates decreasing type-III tunneling current with increasing positive V_G under high RB conditions.

flake partially covers the gate area. Another thin $SnSe_2$ flake was transferred partially on top of WSe_2 (to form the heterojunction) and over the gate on top of the exposed hBN flake left after WSe_2 transfer. The overlapping WSe_2 (p-type) and $SnSe_2$ (n-type) few-layer flakes result in the formation of a pn heterojunction.[24,30] Following the flake transfers, e-beam patterning of source/drain (S/D) contacts on WSe_2 and $SnSe_2$ was carried out, and a Cr (2 nm)/Pt (30 nm)/Au (80 nm) stack was deposited by sputtering to form the S/D contacts. Finally, the as-fabricated device was annealed in ambient conditions at 150 °C for 1 h. The annealing helps in d-orbital hybridization of Pt with WSe_2, thereby lowering the S/D contact resistance for improved p-type conduction.[10] This completed the fabrication process of a gated $WSe_2/SnSe_2$ pn heterojunction diode. A schematic of the device along with the bottom gate and top S/D contacts and an optical microscope image are shown in Figure 1a and b, respectively. Figure 1c shows the equilibrium energy band diagrams of individual WSe_2 and $SnSe_2$ flakes before forming the heterojunction.[6,31] This shows a near-broken type-III band alignment to start with. Thicknesses of the hBN, WSe_2, and $SnSe_2$ flakes were determined to be 21, 9.4, and 25 nm, respectively, using atomic force microscopy scans as shown in Figure S1 in the Supporting Information. It should be noted that the choice of WSe_2 as the bottom layer and $SnSe_2$ as the top layer is determined by good modulation of the WSe_2 FET current and insignificant modulation of the $SnSe_2$ FET current with applied gate voltage (see Figure S2a,b, Supporting Information). Modulation of the FET current, which is proportional to the effective channel carrier density, or doping, plays a key role in the pn heterojunction device performance, as discussed in detail in the next section. Further, Raman spectra were collected for the individual materials as well as for the heterojunction. Figure 1d confirms the formation of a heterojunction, as it displays the presence of peaks belonging to WSe_2 as well as $SnSe_2$ in the spectrum collected from the heterojunction region.

Dark Current Characteristics. First, we have characterized the individual WSe_2 and $SnSe_2$ FETs to establish their p- and n-type behavior, respectively. The transfer characteristics of WSe_2 and $SnSe_2$ are shown in Figure S2 in the Supporting Information, under applied drain bias (V_D) of 2 and 0.5 V (W1 for WSe_2 or S1 for $SnSe_2$) with a grounded source terminal (W2 or S2). With a current ON/OFF ratio of 10^8 and ON state at negative gate voltage (V_G), WSe_2 shows (i) good drain current (I_D) modulation (indicating good carrier modulation) with V_G and (ii) dominant p-type conduction. On the other hand, $SnSe_2$ shows insignificant modulation in current with V_G and dominant n-type conduction. This is due to the degenerate n-doping of $SnSe_2$.[30−32] Thus, the stack of p-WSe_2 and n-$SnSe_2$ constitutes a pn heterojunction. Further, as shown in Figure S2c, in the Supporting Information, under equilibrium, the valence band maximum (VB_{max}) of WSe_2 stays close to the conduction band minimum (CB_{min}) of $SnSe_2$.[24,30] This forms a near-broken gap pn heterojunction. The output characteristics (I_D - V_D) of the heterojunction at different gate voltages under dark condition are shown in Figure 2, center plot. Here, the drain voltage is

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applied at the $SnSe_2$ end with the WSe_2 source terminal being grounded. To avoid drain bias-dependent Schottky barrier modulation at the interface between semiconducting WSe_2 and its metal contact, the drain voltage is applied on the metal contact to degenerately doped $SnSe_2$. As V_D is applied at the $SnSe_2$ (n-type) end, negative voltage at the drain terminal corresponds to forward bias (FB) and positive voltage defines reverse bias (RB) operation of the device. Depending on different V_G and V_D conditions, the $I_D - V_D$ plot can be divided into four distinct sections as marked in Figure 2, center plot. These sections correspond to different interface band alignments resulting from the modulation in carrier concentration by means of electrostatic gating. It can also be noted that as the gate bias changes from −1.5 to 1.5 V, there is a transition from p−n^+ to n−n^+ configuration; however, the direction of the built-in electric field at the heterointerface remains unchanged.

In section 1, for a fixed applied FB (0 V > V_D > −1 V), I_D drops drastically after V_G = −1 V (by four orders in between V_G = −1 V and −0.5 V) as V_G changes from negative to positive voltage. This change in I_D is explained with the help of qualitative band diagrams shown in section 1 of Figure 2. In section 1, when a large negative V_G is applied at the gate terminal, WSe_2 becomes highly p-type, whereas $SnSe_2$ remains highly n-doped. This is because $SnSe_2$ is degenerately doped, and it sees less effect of V_G since it is placed on top of WSe_2. Under this condition, the $WSe_2/SnSe_2$ interface has a type-III band alignment (broken band), such that the $SnSe_2$ CB_{min} is placed below WSe_2 VB_{max}. This leads to direct BTBT of electrons from the $SnSe_2$ conduction band (CB) to the WSe_2 valence band (VB) and a high forward tunneling current under negative V_D. However, when V_G is changed to less negative (> −0.5 V) or positive values, WSe_2 doping transitions from highly p-type to light p-type or n-type. This leads to type-II band alignment at the interface, as shown in Figure 2, section 1 (V_G = −0.5 V). Under this condition, over-the-barrier conduction of electrons from the $SnSe_2$ CB to the WSe_2 CB becomes more probable. Due to the high barrier height encountered by electrons at the interface, very few of them from the $SnSe_2$ CB can reach the WSe_2 CB, and hence the current drops sharply by four orders of magnitude as compared to the tunneling current ($V_D \sim -0.7$ V). Next, in section 2 of Figure 2, center plot, for a high FB voltage (V_D < −1 V) I_D increases as V_G becomes more and more positive. As shown in the Figure 2, section 2, band diagrams, when V_G changes from 0.5 to 1.5 V, WSe_2 doping changes toward more and more n-type, and $SnSe_2$ stays n-doped. This results in a gradual decrease in effective barrier height (for electrons from the $SnSe_2$ CB to the WSe_2 CB) at the interface. Hence, the dark current increases gradually under high FB with increasing V_G. The over-the-barrier thermionic current is characterized by a large slope of nearly 600 mV/decade.

Under small RB (0 V > V_D > 0.5 V), I_D increases with an increase in V_G from 0 to 1.5 V, as shown in Figure 2, center plot, section 3. I_D is determined mainly by electron conduction from the WSe_2 CB to the $SnSe_2$ CB for these voltage conditions as shown in Figure 2, section 3, band diagrams. Therefore, as WSe_2 becomes more and more n-type with increasing V_G, there is enhanced electron transport from WSe_2 to $SnSe_2$, thereby increasing I_D. Section 4 in Figure 2, center plot, depicts a sharp decrease in tunnel current as V_G moves to more and more positive values. This is also explained using Figure 2, section 4, band diagrams. As V_G increases to a more positive value, the WSe_2 Fermi level shifts toward its CB. This results in a shift from type-III towards type-II band alignment and a decrease in separation between the WSe_2 VB and the $SnSe_2$ CB. Therefore, the overlap window for tunneling becomes smaller, which leads to a reduced tunnel current, as shown by the relative thickness of the arrows in Figure 2, section 4, band diagrams (typically for V_D > 1 V). Along with the decrease in tunneling current, the cut-off voltage for the onset of tunneling ($V_{D,cut\text{-}off}$) shifts to higher V_D as V_G increases. This is shown in detail in Figure S3, in the Supporting Information. It is worth noting that, under RB (positive applied V_D), with the same type-III band alignment as discussed in section 1 above, a larger tunneling current is observed (I_D at V_D = 2 V > I_D at V_D = −2 V). In this case electrons tunnel from the WSe_2 VB to the $SnSe_2$ CB, and the relatively higher tunnel current under RB than under FB resembles a backward diode[30] with a maximum on/off rectification of more than five orders under V_G = −0.5 V. This is likely due to the participation of a greater number of electrons in the tunneling from the WSe_2 VB to the $SnSe_2$ CB. Under RB, as the RB voltage increases, the $SnSe_2$ Fermi level goes down in energy with respect to the WSe_2 Fermi level. Therefore, the difference between the WSe_2 and the $SnSe_2$ Fermi level increases. This in turn gives rise to an increased broken gap window for tunneling and helps a greater number of electrons from the WSe_2 VB to take part in tunneling conduction.[23] To confirm type-III tunneling conduction, temperature-dependent $I_D - V_G$ (250 to 77 K) measurements of the heterostructure were carried out (see Figure S4a,b, Supporting Information). The extracted values of SS shown in Figure S4c,d in the Supporting Information show a weak dependence on temperature. This data reinforces tunneling conduction under high negative V_G for both V_D = 2 V (RB) and V_D = −2 V (FB).[24] In summary, the dark characteristics show that the heterodiode band alignment (current transport) can be easily tuned between type-III (tunneling) and type-II (thermionic) using either the gate or the drain bias.

Interface Study Using Density Functional Theory. To understand the nature of band alignment at the $WSe_2/SnSe_2$ heterojunction, first-principles based density functional theory (DFT) calculations using a generalized gradient approximation (GGA) and incorporating van der Waals corrections were performed. In line with the experimental heterostructure comprising few-layer flakes of individual materials, 2L $SnSe_2$ and 2L (and 3L) WSe_2 were used. A hexagonal heterostructure supercell was constructed by stacking $\sqrt{3} \times \sqrt{3}$ units of $SnSe_2$ rotated by 30° on top of 2 × 2 units of WSe_2; the resulting configuration yielding a very low strain (0.36%) was split equally between the two materials. The thickness-dependent band structure diagrams of WSe_2 and $SnSe_2$ are shown in Supporting Information 1, which agree well with reported literature.[33,34] The calculated band structure of 2L WSe_2/2L $SnSe_2$ heterostructure with spin−orbit coupling (SOC) in Figure 3a shows an overlap between the energy levels at the conduction band minimum (at **M**) and valence band maximum (at **K**), with a DFT-GGA calculated overlap energy window of 106 meV. A similar picture is seen in the thicker 3L WSe_2/2L $SnSe_2$ heterostructure (Figure S7, Supporting Information). The VB_{max} is comprised of 5*d* orbitals of WSe_2 while the CB_{min} is made up of the 5*s* and 5*p* orbitals of $SnSe_2$.

To mimic the experimentally supplied gate bias, a transverse electric field was applied in our computations. In the 2L/2L structure, under increasing negative electric field (direction from $SnSe_2$ to WSe_2), the energy window for overlap states

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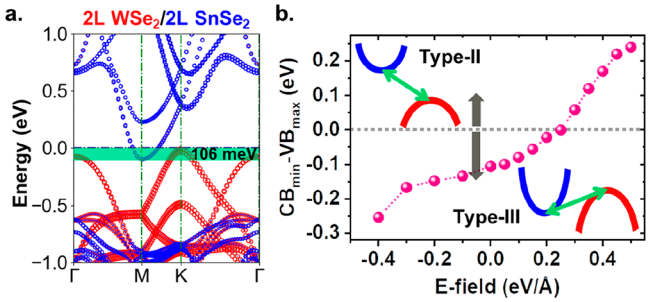

Figure 3. Electric field dependent DFT calculated $WSe_2/SnSe_2$ interface band structure. (a) Calculated band structure of 2L WSe_2/2L $SnSe_2$ heterostructure demonstrating an energy overlap of 106 meV between the conduction band minimum (from $SnSe_2$, in blue) and valence band maximum (from WSe_2, in red). (b) Evolution of energy overlap/difference between the valence band maximum and conduction band minimum with electric field. The interlayer energy levels around the Fermi energy switch from overlap states (type-III) to gapped states (type-II) with increasing electric field.

increases, which could lead to increased tunneling transport (type-III). Whereas, upon reversing the direction of the electric field, the WSe_2 VB states are pulled down in energy leading to the appearance of a bandgap of type-II nature. The tunability of the overlap energy window with electric field is shown in Figure 3b.

Steady State and Temporal Photocharacteristics. Photoresponse of the pn heterojunction was measured under 532 nm laser illumination. The laser incidence was optimized such that only the device junction area was illuminated. Photocurrent (I_{ph}) was extracted using $I_{ph} = I_{light} - I_{Dark}$ (the difference between I_{light} and I_{Dark}), where I_{light} is the device current under illumination and I_{Dark} is the device current measured under dark. Figure 4a shows I_{ph} vs V_D data, and Figure S8a, in the Supporting Information, shows the output characteristics (I_{light} vs V_D), at 25 mW/cm^2 laser intensity under 532 nm illumination for varying V_G. Under both forward and reverse bias conditions corresponding to tunneling regimes under dark (V_G is highly negative), I_{ph} is negative, i.e., I_{light} is less than I_{Dark}. It is worth noting that, under RB for certain V_G conditions (e.g., V_G = 0 and 0.5 V), I_{ph} is positive for low positive V_D and turns negative when V_D is higher, as shown in Figure 4a, inset. The correlation between the change in drain current and heterointerface band alignment upon illumination at various biasing conditions is depicted via qualitative band diagrams in Figure S8b in the Supporting Information.

Further, Figure 4b and its inset clearly depict both negative and positive I_{ph}. The occurrence of negative I_{ph} under tunneling regime for fixed applied V_D is marked through points 1 (dark) and 2 (illumination) in Figure 4b, and corresponding band diagrams are shown in Figure 4c. The band diagrams depict that a substantial generation of electron−hole (e−h) pairs in WSe_2 under illumination shifts its Fermi level from near the VB toward midgap.[35,36] Supporting Information 2 presents a detailed calculation of photocarrier generation under the illumination of 25 mW/cm^2 laser intensity, which further supports the Fermi level shift. This effectively reduces the band overlap for tunnel conduction of electrons from the WSe_2 VB to the $SnSe_2$ CB. Therefore, fewer electrons are available for conduction under BTBT, which in turn decreases the I_D upon illumination. Additionally, the steep change in current with a very small change in RB voltage, as depicted in the current−voltage slope in Figure 4b (200 mV/dec), leads to a large negative I_{ph}, when measured at fixed V_D. Similar to the dark characteristics discussed in Figure 2, section 4, where the

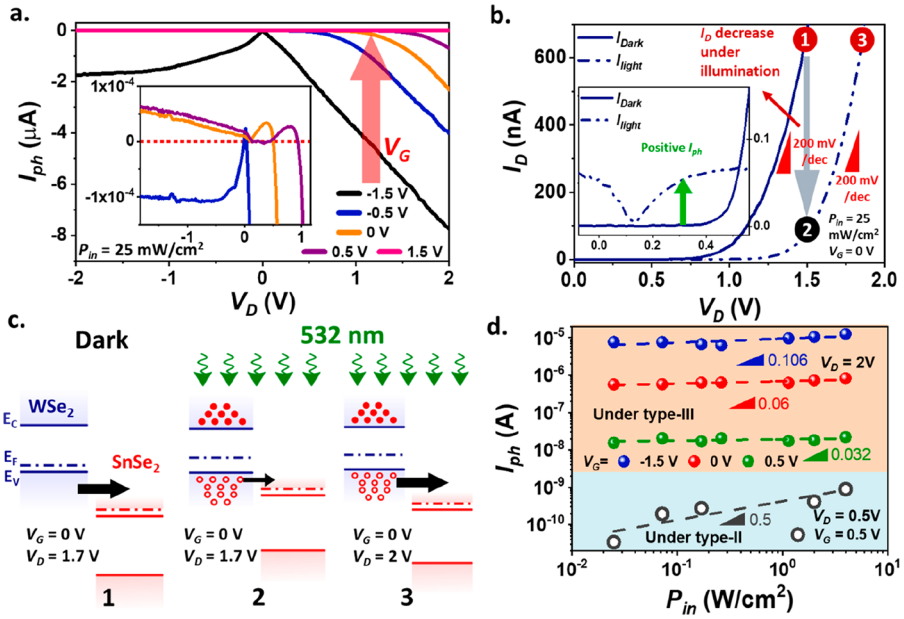

Figure 4. Steady state response and $WSe_2/SnSe_2$ band alignment under illumination. (a) Photocurrent vs V_D under different gate biases at 532 nm illumination for the $WSe_2/SnSe_2$ heterostructure. Inset (plotted on the same scale) shows positive to negative transition of I_{ph}. (b) Magnified output characteristics showing comparison of dark and light current at V_G = 0 V under high V_D type-III biasing whereas the inset (plotted on same scale) depicts the low V_D type-II condition. (c) Heterostructure band diagrams under dark and illumination corresponding to points 1, 2, and 3 in (b) showing a shift in the WSe_2 Fermi level due to photocarrier generation and hence a higher V_D needed to recover the tunnelling current. (d) Photocurrent dependence on incident laser light intensity under type-III and type-II operating regimes highlighting the difference in slopes for the two conditions.

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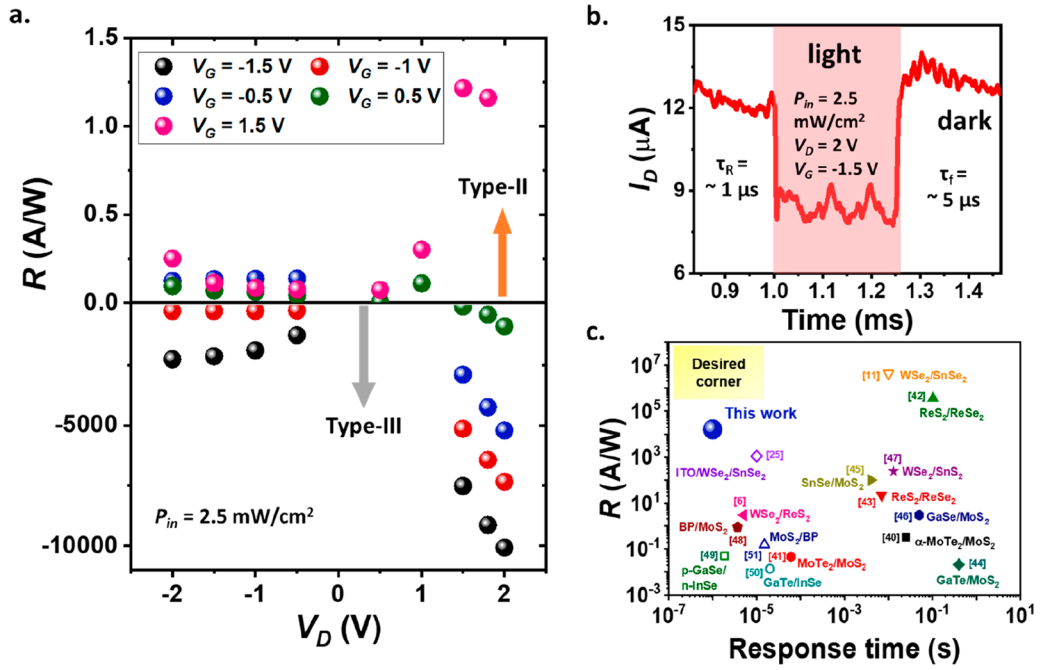

Figure 5. Photoresponsivity, response time, and benchmarking of device performance parameters. (a) R versus V_D showing positive R for type-II and negative R for type-III conduction. (b) Photoswitching characteristic under 2.5 mW/cm² laser intensity and 2 kHz input light frequency showing a fast response time of ∼1 μs and fall time of ∼5 μs. (c) Benchmarking of responsivity and response time values of various reported vdW photodetectors with this work.[40,6,41−51]

tunnel $V_{D,\text{cut-off}}$ was seen to shift due to gate bias-driven change in band alignment, it is seen to shift toward higher V_D values upon illumination as well. This is due to photogeneration of e−h pairs in WSe_2, which causes a shift in the interface band alignment. Figure S9, in the Supporting Information, shows the variation in $V_{D,\text{cut-off}}$ under RB, as a function of V_G and illumination, and the difference between the $V_{D,\text{cut-off}}$ under light and dark ($\Delta V_{D,\text{cut-off}}$) with P_{in}. Due to the shift in $V_{D,\text{cut-off}}$, point 3 in Figure 4b shows that, under illumination, at a slightly higher V_D, I_D recovers to the dark current level (similar to point 1). This is because, at higher RB, the $SnSe_2$ Fermi level along with its VB and CB are pulled down in energy with respect to the WSe_2 Fermi level. This restores the overlap tunnel window, and the tunneling current increases. The positive I_{ph} observed under low RB, as shown in the Figure 4b inset when the device is in type-II regime, is due to photocarrier separation under depletion electric field, which is shown using band diagrams in Figure S10, in the Supporting Information. The positive to negative change in I_{ph} upon illumination with V_D variation for certain V_G values again reinforces the type-II to type-III transition in band alignment with change in V_G and V_D.

It should be noted that since $SnSe_2$ is degenerately doped,[23,30−32] there is no significant modulation in its Fermi energy level upon illumination, as discussed in detail in the Supporting Information 3. Figure 4d shows the dependence of I_{ph} on incident optical power (P_{in}) for type-III (tunneling, high V_D = 2 V) and type-II (over the barrier, low V_D = 0.5 V) conduction regimes. The variation in I_{ph} against P_{in} is small under tunneling conduction, as can be observed from the slopes in the green shaded region of Figure 4d (0.106, 0.06, and 0.032 for V_G = −1.5, 0, and 0.5 V respectively). A similar observation is also reported by Tao et al. for photoconduction under tunneling in an n-Si/MoS_2/Gr system.[37] I_{ph} is positive under type-II configuration as the current is contributed by over-the-barrier conduction of photogenerated carriers. I_{ph} increases as the number of photogenerated carriers increases with increasing P_{in}, resulting in a significant slope of 0.5. The sublinearity is due to the presence of trap states in both materials that cause significant band-to-band recombination of photogenerated carriers before they are collected by the contacts.[38,39] It is also worth noting the substantial improvement (10^4 × at 25 mW/cm²to 10^3 × at 5.4 W/cm²) in I_{ph} magnitude between type-II (V_G = 1.5 V) and type-III (V_G = −1.5 V) regimes for the same drain voltage (V_D = 0.7 V) (see Figure S12, Supporting Information). This clearly underscores the advantage of a type-III photodiode for achieving high R. Figure S13 in the Supporting Information shows similar bias-dependent negative (under type-III) and positive (under type-II) I_{ph} for three different devices, thereby establishing the repeatability of the results demonstrated in this study.

Figure 5a shows the extracted responsivity values from the steady state I_{ph} data measured under 25 mW/cm² laser intensity, using the relation $R = \frac{I_{ph}}{P_{in}}$. The I_{ph} data at 2.5 mW/cm² is presented in Figure S14, in the Supporting Information. High I_{ph} under the tunneling regime leads to high maximum negative R values of ∼2 × 10^4 A/W and ∼200 A/W under reverse and forward bias, respectively. Additionally, the modulation in polarity of R with V_G as well as V_D shows controlled switching between multiple states, which could be further exploited for multi-bit memory and logic devices.

Temporal measurements were carried out for large negative I_{ph} in the strong tunneling regime (V_D = 2 V and V_G = −1 V) to ascertain the speed of operation. The photoswitching characteristics were obtained under 2.5 mW/cm² incident laser intensity with a laser switching frequency of 2 kHz. High I_{ph} values with very fast response time (τ_R) of ∼1 μs and fall time of ∼5 μs were obtained as shown in Figure 5b. Response and fall times are measured using the standard definition of rise and

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ACS Nano 2022, 16, 4578−4587

fall from 10 to 90% and 90 to 10% of the maximum I_{ph} value, respectively.[52] Additionally, Figure S15 in the Supporting Information shows a temporal photoresponse under tunneling for different V_G values applied for the same switching frequency. Similar response times (~1 μs) for all voltage conditions are observed. It is well-known that a tunnel device can switch in the GHz limit.[53] Interlayer charge carrier tunneling time is reported to be on the order of picoseconds for vdW heterostructures.[54] Therefore, the speed of the device used in this study is likely limited by the lateral transport of carriers (electrons) from the (i) WSe_2 (source) contact to the heterointerface, due to bound state electron transport through WSe_2 VB or (ii) from heterointerface to the $SnSe_2$ (drain) contact via the $SnSe_2$ CB, which contributes to the series resistance in the diode current. Hence, the speed can be improved further by narrowing the distance between the source/drain contacts from the heterointerface and by reducing the contact resistance.[38]

The calculated EQE of the device is obtained as $\sim 4 \times 10^4$ %. The shot noise dependent ($S_N = \sqrt{2qI_{dark}}$) specific detectivity (D^*) of the device is calculated to be 2.15×10^{12} Jones, where q is the charge of an electron. We have also obtained the NEP of a similar $WSe_2/SnSe_2$ heterostructure using flicker noise measurements to be 2.12×10^{-13} W/$\sqrt{\text{Hz}}$. From NEP, flicker noise-limited D^*, calculated as $D^* = \frac{\sqrt{(A)}}{NEP}$ where A is the area of the device, is found to be 9.12×10^9 Jones. Measured flicker noise and extraction of NEP is shown in Supporting Information Figure S16. Further, the spectral photoresponse measured for the device from 490 to 850 nm wavelength shows a broadband photoresponse of the photodetector (see Supporting Information Figure S17).

Finally, we have benchmarked our data (R vs τ_R) against high performance photodetection studies based on vdW heterostructures reported to date (see Figure 5c). Heterojunction photodiodes as well as phototransistors formed using stacked vdW materials have been used in this plot. The very high R (2×10^4 A/W) at a response time of ~1 μs and fall time of ~5 μs reported in this work, stands out among a large number of high-performance 2D heterostructure photodetectors. In addition, this is also one of the fastest vdW material-based photodetectors with high negative photoresponsivity as shown in Table S1, in the Supporting Information.

CONCLUSION

This work demonstrates a high-performance tunnel photodiode with ultrahigh responsivity and high speed. Leveraging the benefit of a near-broken bandgap under equilibrium, the device was operated in both type-II (staggered) and type-III (broken) interlayer bandgap configurations as a function of V_G and V_D, and the latter was further confirmed by temperature-dependent I_D-V_G measurements. A comprehensive DFT study on the electronic band structure at the heterointerface affirmed the electric field dependent modulation between type-III and -II band alignment. At room temperature, I_D-V_D data of the device shows a backward diode-like nature with a high rectification ratio of $\sim 10^5$. A thorough study under illumination with varying incident power and different V_G and V_D conditions showed a positive value of R under type-II operation that was enhanced by nearly $10^4\times$ to a large negative R value under type-III operation. Large negative responsivity of 2×10^4 A/W with a short response time of ~1 μs and a very fast fall time of ~5 μs achieved under the type-III tunneling regime along with bias-dependent switching of photocurrent polarity makes this tunnel photodiode promising for future optoelectronic applications ranging from optical communication to multi-bit memory and logic devices.

EXPERIMENTAL PROCEDURE

Device Fabrication. A single side polished 4 inch p^+-Si wafer with 285 nm SiO_2 grown on top was used as the substrate. Gate contact was patterned first on top of the Si/SiO_2 wafer by electron beam lithography (EBL, Raith 150-Two). This was followed by metal (Cr 2 nm/Au 30 nm) deposition (AJA, ATC sputter system) and lift-off. The length and width of the gate contact were 30 and 20 μm, respectively. Bulk and single-crystal WSe_2 and hBN were purchased from SPI Supplies. $SnSe_2$ was purchased from 2D Semiconductors. An hBN flake was exfoliated using the micromechanical exfoliation technique with 3M magic scotch tape. The hBN flake was then transferred from the scotch tape onto a polydimethylsiloxane (PDMS) stamp. The PDMS stamp was fixed onto a glass slide, and the glass slide was attached to a micromanipulator. The hBN flake was transferred selectively on top of the prefabricated gate structure using the micromanipulator under an Olympus BX-63 microscope. During the transfer process, the Si/SiO_2 substrate with its gate pattern was placed on top of a microheater. After the hBN was aligned and placed on top of the gate pattern, the entire structure—consisting of the Si/SiO_2 substrate and the hBN flake along with the PDMS stamp and the glass slide, was heated to 60 °C to weaken the adhesion between the PDMS stamp and the hBN flake. The temperature was then allowed to come down to 50 °C to release the glass slide and the PDMS stamp from the Si/SiO_2 substrate, leaving behind only the hBN flake on top of the gate pattern. The same transfer process was followed for aligning and placing a few-layer WSe_2 flake on top of the hBN flake, followed by an $SnSe_2$ flake on top of the WSe_2 and hBN flakes, to form a $WSe_2/SnSe_2$ heterostructure. The WSe_2 flake was placed in such a way that it partially covered the patterned gate area without touching the extended gate leads. The $SnSe_2$ flake was placed in such a way that part of the flake came on top of WSe_2 to make a heterojunction and the rest was placed on top of the hBN gate, within the patterned gate contact area. Next, a total of four contacts were patterned using EBL, two each on top of the WSe_2 and $SnSe_2$ flakes. Finally, contact sputter metallization (Cr 2 nm/Pt 30 nm/Au 80 nm) and lift-off were carried out to complete the device fabrication.

Device Characterization. Before optoelectrical characterization, the device was wire bonded to a PCB. All electrical measurements were done in ambient conditions under a BX-63 Olympus microscope using a Keysight B1500A semiconductor device analyzer. The photoresponse measurements were carried out using a NKT SuperK EXU-6 laser. Steady-state photoresponse was measured using Keysight B1500A, and the temporal response was measured using a 4 GHz Keysight DSOS404A oscilloscope and current probe (Keysight 2825A). Input laser power was modulated from off to on using square pulses of 1 V peak-to-peak to the laser power controller unit from an Agilent 33220A function generator. The laser was incident on the device through the objective lens of the BX-63 Olympus microscope. Input optical power was varied by inserting suitable optical density filters from HOLMARC in the path of the 532 nm laser beam.

Density Functional Theory Calculations. All of the atomistic simulations were implemented using the Vienna Ab initio Simulation Package (VASP). The generalized gradient approximation of Perdew—Burke—Ernzerhof (PBE) was used to describe the exchange correlation effects and projector augmented wave (PAW) pseudopotentials were employed to account for the interactions between the frozen core and valence electrons.[55,56] The dispersion corrected DFT-D3 method was invoked to introduce van der Waals interaction between the two materials.[57] For the structural optimizations, a plane wave cut-off of 400 eV and a Γ-centered k-points grid of $7 \times 7 \times 1$ were used. The self-consistent calculations included the effects of spin—orbit coupling and used an energy cut-off of 400 eV along with a

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denser k-points grid of 9 × 9 × 1. The optimizations were carried out until the energy convergence of 0.1 meV was reached and the Hellman−Feynman forces were less than 0.01 eV/Å. Sufficient vacuum (>15 Å) was incorporated in all supercells along the out-of-plane direction to avoid spurious interactions between adjacent periodic images. Bandgaps typically underestimated by GGA-PBE were calculated using the hybrid HSE06 scheme[58] using the maximally localized Wannier functions in the Wannier90 package.[59] The effect of a transverse electric field was performed by VASP by introducing an artificial dipole sheet in the supercell. VASPKIT tool[60] was used for postprocessing of the calculated data. VESTA was used to visualize the crystal structures.

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acsnano.1c11110.

AFM images, transfer characteristics of WSe_2 and $SnSe_2$, temperature dependent transfer characteristics of the heterostructure, extendend discussion on DFT methodology, output characteristics band diagrams under light, calculation of photon density at 5 nW laser power and WSe_2 channel carrier density, shift in tunneling cutoff voltage with gate bias and under illumination, photoresponse of $SnSe_2$ FET, comparison of positive and negative photocurrent with light intensity, output characteristics under dark and illumination of multiple similar devices, photocurrent vs V_D at different V_G values, response time at different V_G values, flicker noise data and NEP calculation, and spectral response and benchmarking table of responsivity and speed for 2D material based photodetectors (PDF)

AUTHOR INFORMATION

Corresponding Author

Saurabh Lodha − *Department of Electrical Engineering, IIT Bombay, Mumbai 400076, India;* orcid.org/0000-0002-0690-3169; Email: slodha@ee.iitb.ac.in

Authors

Sayantan Ghosh − *Department of Electrical Engineering, IIT Bombay, Mumbai 400076, India*

Abin Varghese − *Department of Electrical Engineering, IIT Bombay, Mumbai 400076, India; Department of Materials Science and Engineering, Monash University, Clayton, Victoria 3800, Australia; IITB-Monash Research Academy, IIT Bombay, Mumbai 400076, India;* orcid.org/0000-0002-6241-9080

Himani Jawa − *Department of Electrical Engineering, IIT Bombay, Mumbai 400076, India*

Yuefeng Yin − *Department of Materials Science and Engineering, Monash University, Clayton, Victoria 3800, Australia*

Nikhil V. Medhekar − *Department of Materials Science and Engineering, Monash University, Clayton, Victoria 3800, Australia;* orcid.org/0000-0003-3124-4430

Complete contact information is available at: https://pubs.acs.org/10.1021/acsnano.1c11110

Notes

The authors declare no competing financial interest.

The data sets generated/analyzed during this study are available from the authors on reasonable request.

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