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ARTICLE

Pick-and-Place Transfer of Arbitrary-Metal Electrodes for van der Waals Device Fabrication

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Cite This: *ACS Nano* 2025, 19, 3579–3588

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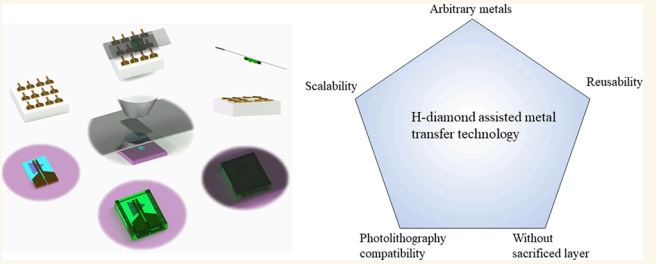
ABSTRACT: **Van der Waals electrode integration is a promising strategy to create nearly perfect interfaces between metals and 2D materials, with advantages such as eliminating Fermi-level pinning and reducing contact resistance. However, the lack of a simple, generalizable pick-and-place transfer technology has greatly hampered the wide use of this technique. We demonstrate the pick-and-place transfer of prefabricated electrodes from reusable polished hydrogenated diamond substrates without the use of any sacrificial layers due to the inherent low-energy and dangling-bond-free nature of the hydrogenated diamond surface. The technique enables transfer of arbitrary-metal electrodes and an electrode array, as demonstrated by successful transfer of eight different elemental metals with work functions ranging from 4.22 to 5.65 eV. We also demonstrate the electrode array transfer for large-scale device fabrication. The mechanical transfer of metal electrodes from diamond to van der Waals materials creates atomically smooth interfaces with no interstitial impurities or disorder, as observed with cross-section high-resolution transmission electron microscopy and energy-dispersive X-ray spectroscopy. As a demonstration of its device application, we use the diamond transfer technique to create metal contacts to monolayer transition metal dichalcogenide semiconductors with high-work-function Pd, low-work-function Ti, and semimetal Bi to create *n*- and *p*-type field-effect transistors with low Schottky barrier heights. We also extend this technology to air-sensitive materials (trilayer 1T' WTe_2) and other applications such as ambipolar transistors, Schottky diodes, and optoelectronics. This highly reliable and reproducible technology paves the way for new device architectures and high-performance devices.**



KEYWORDS: *vdW ohmic contacts, hydrogenated diamond surface, arbitrary transfer of scalable electrodes, low Schottky barrier, Fermi-level depinning, 2D materials*

The advent of van der Waals (vdW) heterostructures has revolutionized materials physics and electronic and optoelectronic device technologies.[1−4] While vdW heterostructures are typically constructed from layered materials held together by vdW forces, integration of conventional materials in such structures is also desirable but carries unique challenges. Conventional metals are often used as electrical contacts and interconnects; however, conventional metal deposition techniques can damage the vdW interface causing undesirable disorder.[5,6] Evaporated metal atoms with high kinetic energy bombard the contact areas during the evaporation, which has been shown to induce significant amounts of damage and defects into vdW semiconductors, which leads the metal-induced gap states (MIGS) or defect-induced gap states (DIGS), resulting in a strong Fermi-level (FL) pinning effect.[7,8] This in turn causes the Schottky barrier height (SBH) to become insensitive to the metal work function, resulting in low-efficiency carrier injection and large contact resistance, which greatly hampers the observation of novel physics and the development of 2D semiconductor-based electronics. To address these challenges,

Received: September 26, 2024
Revised: December 21, 2024
Accepted: December 27, 2024
Published: January 13, 2025

considerable efforts have been devoted to minimizing both FL pinning and contact resistance during the past decade. Forming vdW interfaces between three-dimensional metals (In[9] and Pd[10]) and 2D semiconductors has been demonstrated via precise control of the electron beam evaporation. Growth of buffer layers with low formation energy, such as semimetals (Bi, Sb, and $ZrTe_2$)[11−13] on contact regions before metallization has been demonstrated as another effective strategy of *n*-type ohmic contacts for monolayer MoS_2 in terms of reducing the possible surface defect states, minimizing SBH, and even pushing the contact resistance down to the quantum limitation (42 Ω μm).[12] On the other hand, surface transfer doping the TMDs (MoS_2 and WSe_2) beneath the electrodes by high-electron-affinity transition metal oxides (TMOs) has been reported as an excellent approach to form the *p*-type ohmic contacts down to the cryogenic regime because the TMOs degenerately dope the TMDs but creates minimal defects.[14,15]

An emerging strategy is the pick-and-place mechanical transfer of predeposited metal contacts, which has been demonstrated to maintain the low-energy vdW interaction between metal electrodes and 2D materials, rather than chemical bonding, resulting in an ideal interface and tunable SBH (reaching the Schottky−Mott limit[16]). Graphene on a germanium substrate has proven to be an effective method for assisting electrode transfer onto 2D materials. However, the fragile nature of graphene limits the reusable nature and presents challenges for industrial applications.[17] To overcome this, Zhang *et al.* utilized fluorophlogopite mica, which addressed the fragility issue. Nonetheless, this approach has been limited to specific metals, such as Au, Pt, Pd, and Al.[18] Many of the industry-preferred metals (such as Ti and Cr) show a strong adhesion to the substrates and cannot be picked up easily with the standard dry transfer technologies due the lack of low-energy surfaces for the vdW interface formation between metals and substrates.[16] A few works have attempted to resolve this limitation.[17−20] Sacrificial layers (Se or propylene carbonate (PPC)) were formed on the 2D semiconductors before high-energy metallization to protect the 2D semiconductors. Afterward, the sacrificial layers were removed by an annealing process at elevated temperatures (Se @ ∼350 °C and PPC @ ∼250 °C), and the top metal electrodes collapsed onto the 2D semiconductors.[19,20] However, any sacrificial-layer process adds additional material and the potential for impurities at the vdW interface, which might alter its electronics properties. The additional processing is also undesirable and may be incompatible with other processes. Se deposition still requires a high-energy process, which may be harmful to the monolayer TMDs. The spin-coated PPC method works only with shadow masks because the PPC film is soluble in the common resist developers. Therefore, it is desirable to develop a simple, universal metal electrode fabrication technology that is universally compatible with vdW heterostructure fabrication.

Here, we demonstrate a reliable universal pick-and-place transfer technology for scalable metal electrodes without using any sacrificial layers for future electronics based on 2D materials. Table S1 summarizes several advantages, including the capability to transfer arbitrary metals, elimination of sacrificial layers, scalability, compatibility with photolithography, and reusability, in comparison with recent studies. Polished hydrogenated diamond substrates are utilized as reusable substrates for metal electrode fabrication by standard lithographic techniques. The hydrogenated diamond surface enables transfer of a wide variety of metals; we demonstrate transfer of eight different elemental metals with the work function ranging from 4.22 to 5.65 eV. Due to the low adhesion and dangling-bond-free nature of the hydrogenated diamond surface, prepatterned metals can be easily peeled off by poly(bisphenol A carbonate) (PC) or PPC stamps then aligned and laminated onto 2D semiconductors to form the 2D material-based devices. We characterized the vdW interface between transferred electrodes and 2D semiconductors (WSe_2 and MoS_2) with high-resolution transmission electron microscopy (HRTEM) and observed atomically clean and damage-free interfaces. We demonstrate the utility of the technique by fabricating field-effect transistors from monolayer transition metal dichalcogenides (TMDs) with three diamond-transferred electrodes of different metals (Pd, Bi, and Ti), showing low-SBH contacts in both *n*-type (Bi and Ti for MoS_2) and *p*-type (Pd for WSe_2) operation. This proposed vdW device fabrication technology offers a simple and reliable approach for air-sensitive 2D materials, such as 1T' WTe_2, compared with other reported methods.[21,22] We also extend our diamond transfer technology to few-layer TMDs to demonstrate device applications such as ambipolar transistors, Schottky barrier diodes, and photodetectors. Our work realized vdW contacts for 2D semiconductors with a broad range of metals, as well as minimized the FL pinning effect with a FL pinning factor of ∼0.7 ± 0.2. Moreover, transfer of a large-scale electrode array paves the way for the wafer-scaled device fabrication compatible with the commercialized nanofabrication process.

RESULTS AND DISCUSSION

Prior to the metal contact fabrication, the (100) diamond substrates were polished by a scaif wheel (Technical Diamond Polishing) to minimize the surface roughness down to the sub-nanometer regime. Then, the hydrogen termination was conducted in a Seki6500 diamond deposition reactor, consisting of a 2.4 GHz microwave plasma-assisted chemical vapor deposition chamber. The prepolished diamond samples were loaded onto a polycrystalline diamond-coated molybdenum carrier and exposed to 85 Torr, 4500 W hydrogen plasma, with a H_2 flow rate of 450 sccm at 800 °C. In order to produce a locally smooth surface (avoid the etching pits during the termination) and minimize contamination oxygen in the chamber, two different concentrations of CH_4 were added to the plasma, with an initial flow of 2.1 sccm CH_4 for 1 min during sample heating at the start of plasma exposure, followed by 4.1 sccm for another 1 min. The CH_4 flow was then turned off, and the plasma was slowly extinguished by gradually turning the microwave power to 3200 W over a period of approximately 2 min and then turning it off (Figure S1a). The roughness of the hydrogenated diamond surface has been investigated by atomic force microscopy (AFM) before the metallization. As illustrated in Figure S1b, the polished hydrogenated diamond has been characterized, and the root-mean-square roughness is around 0.32 nm, which suggests no etching pit formation during the hydrogen plasma process, resulting in an excellent smooth surface condition. Another two polished hydrogenated diamonds have been characterized as well, and both of them show low surface roughness (Figure S1c. The low roughness of the hydrogenated diamond surface is critical for the following electrode fabrication and integration in atomically flat vdW heterostructures. As shown in Figure S2a,b, electrode deposition and transfer from a different rough diamond with a high density of etch pits generated during the hydrogen termination result in visible roughness imprinted in the electrode surfaces after

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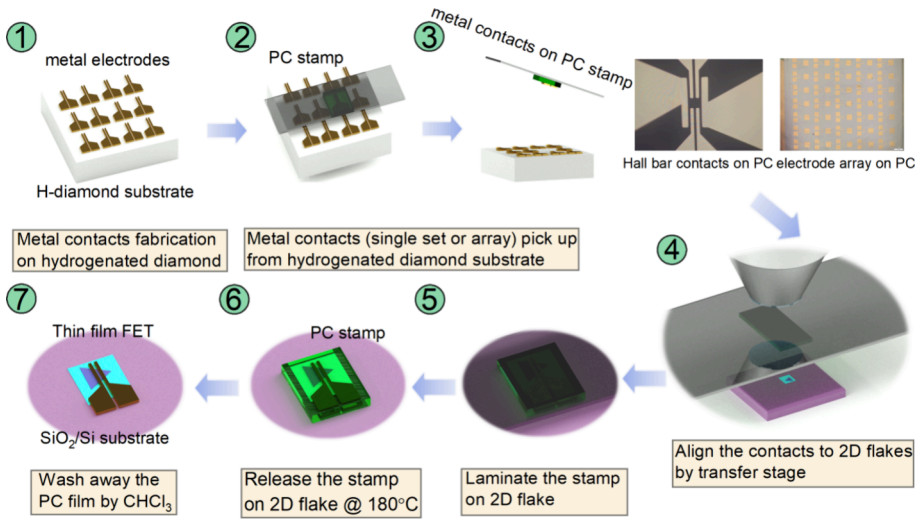

Figure 1. Schematic illustration of hydrogenated diamond-assisted metal electrode transfer for 2D semiconductor device fabrication.

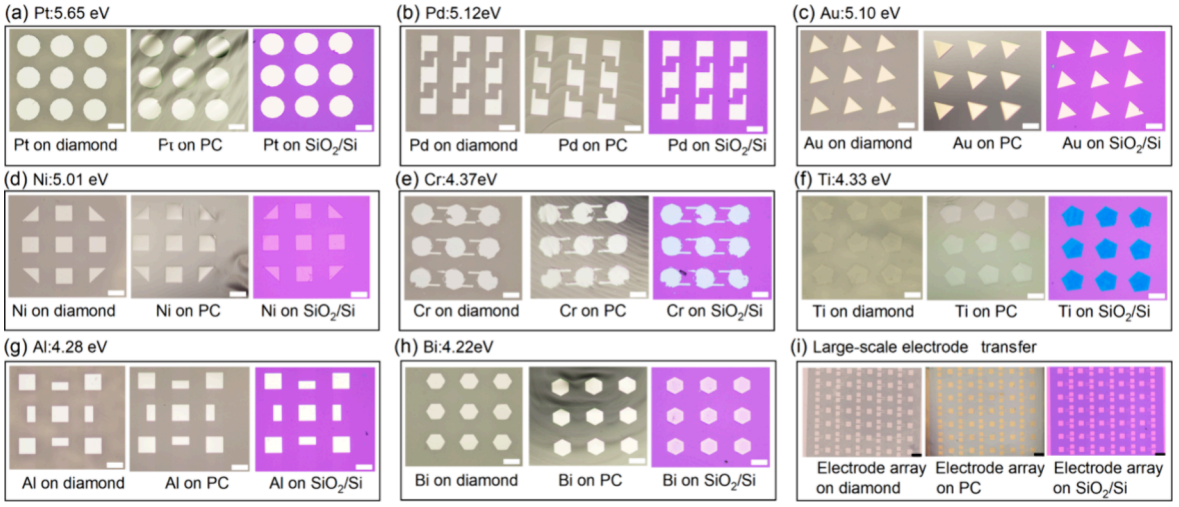

Figure 2. (a–i) Micrographs of metal films (Pt, Pd, Au, Ni, Cr, Ti, Ai, Bi, and electrode array) in various shapes transferred from the same hydrogenated diamond substrate to SiO_2 (285 nm)/Si substrates by the dry transfer method. The white scale bars represent 50 μm. The black scale bars represent 100 μm.

picking up from the rough diamond substrates. The rough electrodes showed greatly reduced adhesion as well as increased the nonuniformity between the contacts and 2D semiconductors after lamination (Figure S2c,d).

Then, metal electrodes were fabricated on polished hydrogenated diamond substrates by conventional photolithography technologies and e-beam evaporation. It should be noted that, after the development of the photoresist before metal deposition, diamond substrates were *in situ* exposed to argon plasma for 2 s to remove possible resist residues. After the lift-off process, the patterned metals on hydrogenated diamonds have been picked up by PC stamps (the PC stamps had been heated up to 150 °C to make the PC film completely touch the metal electrodes and then cooled down to room temperature to achieve the detachment). All steps were performed in a glovebox to minimize the oxidization, especially for low-work-function metals such as Ti, Al, and Bi. The pick-up process was smooth and gentle as shown in the video in the Supporting Information, which can greatly minimize the cracks or folding of metals during the pick-up process. Lastly, the picked-up metals were laminated onto the target 2D semiconductor heterostructures, as illustrated in Figure 1.

In order to demonstrate that this technique is effective for a broad range of metals, eight candidates (from high-work-function metal to low-work-function metal) have been investigated in this work. Figure 2a–h shows optical micrographs of photolithography-patterned metal films (Pt, Pd, Au, Ni, Cr, Ti, Al, and Bi) on the diamond substrate, picked up by PC stamps, and transferred to target SiO_2/Si substrates. All metals can be peeled off from the hydrogenated diamond surface easily and keep their initial geometries without any cracks or folding after landing on the SiO_2/Si substrates. Liu *et al.* reported that metals with the strongest adhesion force (Ni, Ti, and Cr) showed an extremely low releasing yield[16] from hexamethyldisilazane-treated silicon. Here, the diamond-assisted metal pick-up technology shows a very high releasing yield for these three reactive metals due to the low-energy nature of the hydrogenated diamond surface, demonstrating the universal nature of this technology. It should be noted that all eight metal candidates were peeled off of the same diamond, which demonstrates the reusable nature of this technology. This is

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ACS Nano 2025, 19, 3579–3588

because the hydrogenated diamond surface is thermally stable up to ~450 K in the atmosphere.[23] In addition, we measured the surface conductivity of the hydrogenated diamond surface before and after multiple picking-up processes; the sheet resistance of the diamond surface experienced almost no changes (Figure S3), indicating the intact hydrogen termination after repeated pick-up and transfer processes.[23] It should be noted that annealing diamond substrates over 300 °C in the atmosphere will lead to surface oxidation, significantly increasing the surface adhesion to metals and resulting in a very low yield for picking up metals.[24] After rehydrogen terminating the diamonds, the substrates can be reused. We have also shown that the diamond-assisted vdW electrode integration process is highly reproducible and scalable, making it suitable for large-scale 2D device fabrication. In Figure 2i, large-scale (3 mm × 3 mm) patterned electrodes (Cr 5 nm/Au 20 nm) were transferred from hydrogenated diamond to SiO_2/Si by the PC method with nearly 100% yield. In addition, these electrodes' array can also be aligned to the patterned films precisely as shown in Figure S4a,b. We further investigated the yield of picking up the Ti array, Ni array, and Al/Au asymmetric array. All exhibited nearly 100% yield, as shown in Figure S4c. The imperfections observed are attributed to dust particles on either the diamonds or the PC stamps, which can be minimized by conducting all processes in a cleanroom environment. This capability paves the way for the wafer-scale vdW arbitrary-electrode integration for 2D semiconductor device fabrication.[25]

Density functional theory (DFT) calculations were carried out to gain a further understanding of the ultralow surface adhesion energy of hydrogenated diamond, which enables the diamond-assisted metal transfer technology. Here, we have focused on a few representative metals, i.e., Ti, Ni, Cr, and Al, that usually exhibit strong adhesion with substrates such as SiO_2/Si by modeling their interfacial interaction with the hydrogenated diamond surface and comparing that with the SiO_2 substrate as well as a vdW substrate, graphene. The DFT-D3 method was employed to accurately model the vdW force between metals and the hydrogenated diamond C (001) 2 × 1:H surface.[26] To assess the exfoliation feasibility, we defined the exfoliation energy as

$$E_{\text{exfoliation}} = (E_{\text{Metal}} + E_{\text{Substrate}} - E_{\text{Hetero}})/A$$

where E_{Metal}, $E_{\text{Substrate}}$, and E_{Hetero} represent the energies of metals, substrates, and metal/substrate heterostructures. A represents the area of the surface unit cell. Notably, calculated results depicted in Figure 3 illustrate significantly lower exfoliation energies for the selected metals on the hydrogenated diamond surface compared to SiO_2 substrates by more than an order of magnitude. Moreover, the $E_{\text{exfoliation}}$ for metals on hydrogenated diamond is almost independent of the choice of metals, whereas the $E_{\text{exfoliation}}$ for metals on graphene varies with the specific metal used. For example, Ti exhibits strong interactions with graphene (four times higher than that on hydrogenated diamonds) due to possible chemisorption with graphene, as evidenced by the buckled shape of graphene upon relaxation (Figure S5).[27] Additionally, hydrogenated diamond demonstrates a lower $E_{\text{exfoliation}}$ for Al pick-up compared to F-mica.[18] These findings underscore the extremely weak vdW interactions at the interface between metals and hydrogenated diamond regardless of the specific metal used. This behavior is indicative of quasi-vdW epitaxy, consistent with experimental results.

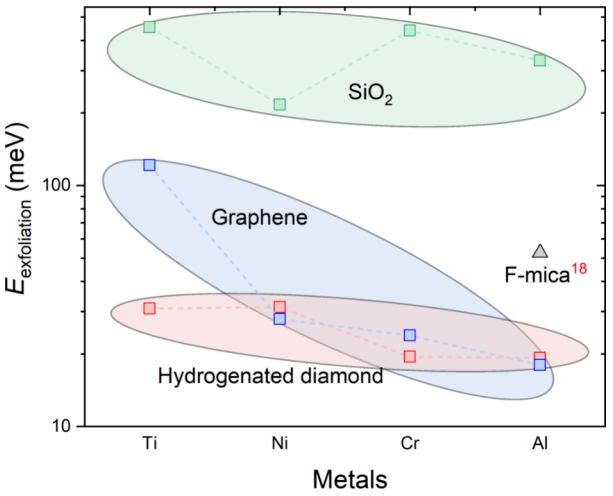

Figure 3. Theoretical calculation of the exfoliation energy for metals Ti, Ni, Cr, and Al on the hydrogenated diamond surface, graphene, F-mica,[18] and SiO_2. The schematic diagrams of the relaxed structures for each metal/substrate combination are shown in Figure S5 in the Supporting Information.

We then utilized diamond transfer technology (Figure 1) to integrate metal contacts on monolayer TMD/*h*-BN vdW heterostructures. We assessed the interface quality through cross-section TEM and energy-dispersive X-ray spectroscopy (EDS) while characterizing the device transport properties at both room temperature and 77 K. According to Figure 4a, the

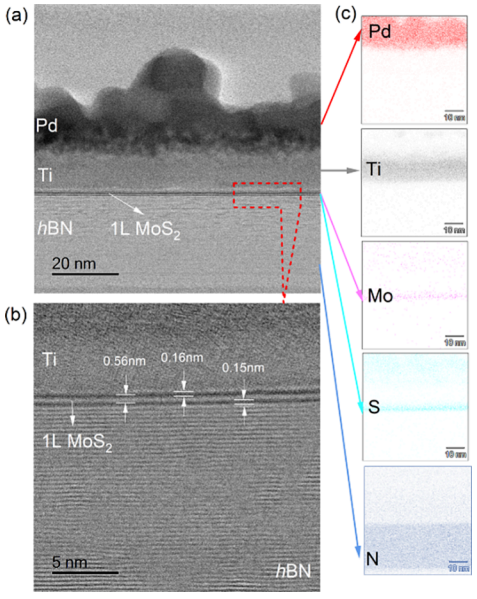

Figure 4. Characterization of the transferred electrodes (Pd/Ti)/monolayer TMD (MoS_2)/*h*BN heterostructures in terms of cross-section STEM using bright-field imaging (a,b) and EDS elemental mapping (c).

monolayer MoS_2 lattice structure is well-retained without any damage, defects, or contaminations (such as residual photo-resist), which is consistent with the literature.[16] Notably, the vdW gaps between metal/TMD and TMD/*h*BN were clearly discernible, as marked in Figure 4b. In a few cross-section TEM images (Figure S6), we find that a few localized bubbles of interstitial material are observed at the metal/monolayer TMD

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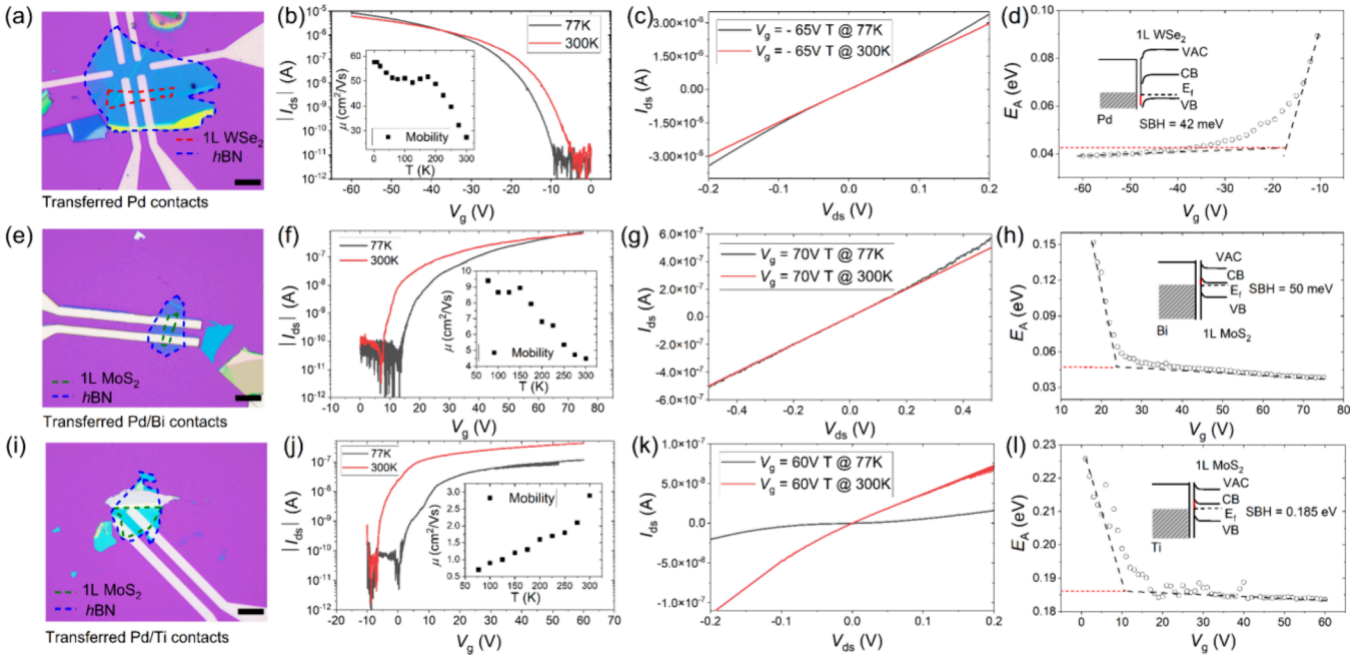

Figure 5. Transport characterization of transferred electrodes on monolayer TMD FETs, including transfer curves, field-effect mobilities as a function of temperatures, output curves at different temperatures (77 and 300 K), and Schottky barrier high analysis. (a) Optical image and (b–d) data for 1L WSe_2 integrated with transferred Pd. (e) Optical image and (f–h) data for 1L MoS_2 integrated with transferred Pd/Bi. (i) Optical image and (j–l) data for 1L MoS_2 integrated with transferred Pd/Ti. The scale bar for each optical image was 10 μm.

interfaces. Eliminating such bubbles through techniques such as postannealing in Ar ambient or vacuum is the subject of future work. Consequently, employing vdW electrodes for contacting 2D semiconductors, especially for monolayer materials, presents a low-energy integration approach compared with conventional methods such as lithography and metallization. This approach significantly reduces the formation of defect states, strain, damage, and contamination associated with the lithography process.

In order to demonstrate the versatility of our technique, we fabricated both *n*-type and *p*-type back-gate 1L TMDs with three sets of transferred metal electrodes: (I) high-work-function metal Pd in contact to 1L WSe_2 (optic image in Figure 5a); (II) semimetal Bi in contact to 1L MoS_2 (optic image in Figure 5e); (III) low-work-function metal Ti in contact to 1L MoS_2 (optic image in Figure 5i). First, the Pd/WSe_2 FET shows typical hole conduction behavior with a high on/off current ratio of $\sim 10^7$. The source-drain current, I_{sd}, with a −65 V gate bias at 77 K exceeded that at room temperature. Two-terminal field-effect mobilities, as depicted in the inset of Figure 5b, increased from 27 to 57 $cm^2/(V\ s)$ as the temperature dropped to 77 K, indicating the good ohmic behavior between metals and TMDs. Output curves (Figure 5c) with a gate bias of −65 V at both 300 and 77K displayed the high linearity, further suggesting the ohmic behavior with low Schottky barrier heights. Regarding the 1L MoS_2 *n*-type FET, we also observed the ohmic behavior between transferred Pd/Bi and 1L MoS_2 in terms of transfer curves (Figure 5f), field-effect mobilities (inset of Figure 5f), and linear output curves (Figure 5g) at both room temperature and 77 K, which is consistent with the reported work.[11] However, the 1L MoS_2 FET with Pd/Ti electrodes shows typical Schottky contact behavior. The source-drain current experiences a reduction during the cooling down process (Figure 5j), and mobilities decrease from 3 to 0.6 $cm^2/(V\ s)$ as shown in the inset of Figure 5j. The *I*−*V* curve at a gate bias of 60 V transitioned from linear at room temperature to nonlinear at 77 K, indicating the presence of a high-energy barrier (Figure 5k). The possible reason might be due to the oxidation of Ti during the transfer process even in glovebox environment. Despite this, all these three devices show high linearity in output curves (Figure S7b,d,f), suggesting the similar SBH at each metal−semiconductor interface, whereas the evaporated contacts often exhibit asymmetric *I*−*V* due to the damage of the crystal lattice during the high-energy metal deposition process (Figure S7a,c,e). Regarding the reproducibility, we fabricated another three similar devices and studied the transport properties as a function of temperature. Pd/1L WSe_2 and Pd/Bi MoS_2 show ohmic behavior down to 77 K (Figure S8a–f), whereas Pd/Ti MoS_2 shows Schottky behavior at low temperature (Figure S8g–i). All three devices show similar performance to the devices discussed in Figure 5, which demonstrates the reproducibility of this contact fabrication technology. In addition, 10 CVD-grown MoS_2 FETs with transferred Pd/Bi contacts were investigated to assess device-to-device variation. All devices exhibited similar transfer characteristics, including two-terminal field-effect mobility, on−off ratio, and threshold voltage (Figure S9), indicating that this proposed technology enables the fabrication of highly reliable and reproducible devices with low device-to-device variation. From Figure S10, the Arrhenius plots for these three devices were further extracted, allowing us to quantitively estimate the SBH for each metal/TMD interface. The detailed calculated SBH values at different gate bias extracted from the Arrhenius plots are plotted in Figure 5d,h,l, separately. Both Pd/WSe_2 and Bi/MoS_2 interfaces show very low SBH, approximately 42 and 50 meV, respectively. These low SBHs are consistent with the linear *I*−*V* curve at low temperatures. The high SHB (185 meV) between Ti and MoS_2 explains the nonlinear *I*−*V* behavior at a low temperature. Notably, we demonstrate that different work function-transferred metal electrodes can form low SBH to

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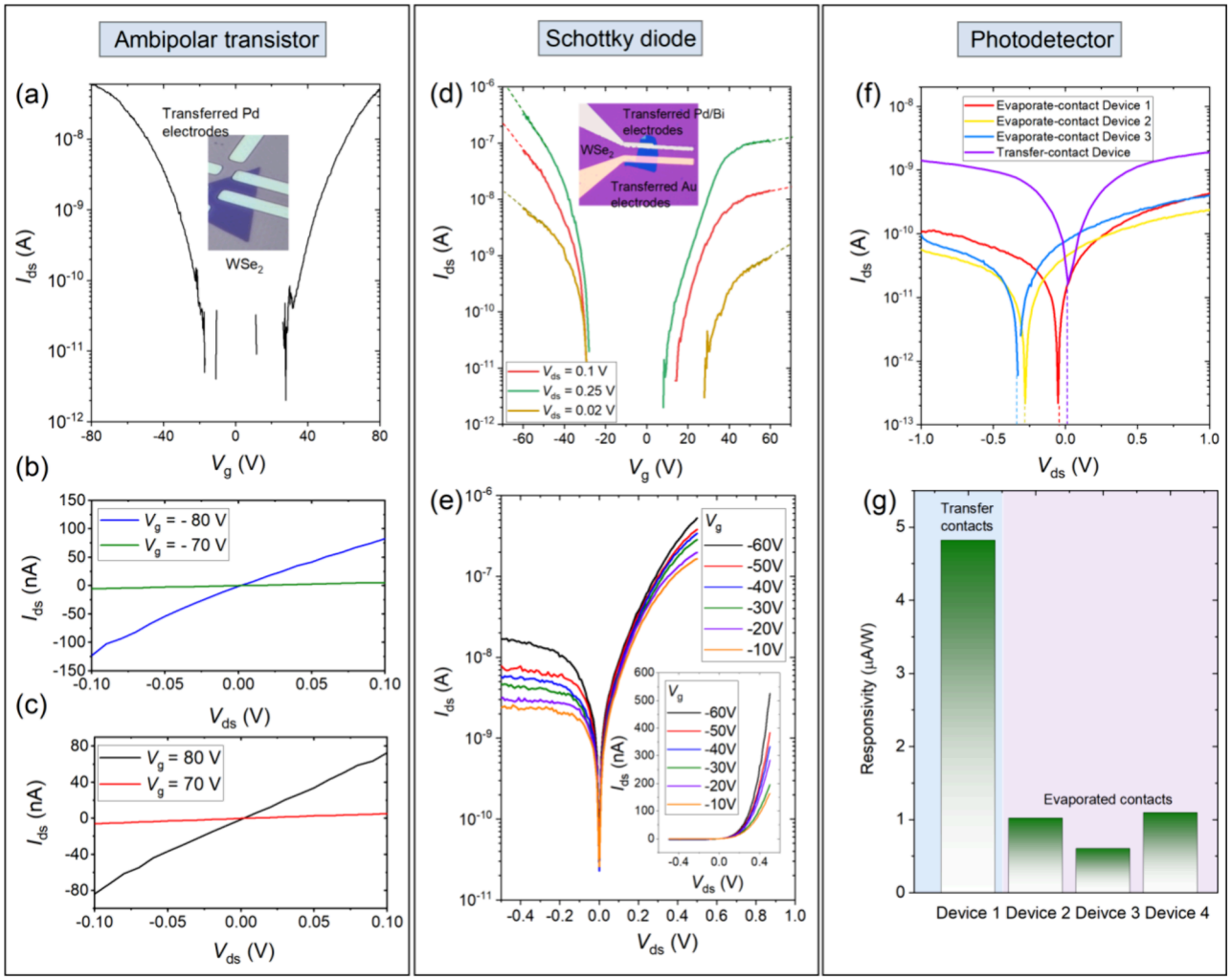

Figure 6. Transferred electrodes for few-layer TMDs applied to create an ambipolar FET, a Schottky barrier diode, and a photodetector. (a–c) Transfer characteristics (a) and output characteristics (b,c) in the *n*-type (b) and *p*-type (c) regimes of ambipolar few-layer WSe_2 FETs with transferred Pd contacts. (d,e) Transfer (d) and output (e) characteristics of a Schottky barrier diode created by contacting few-layer WS_2 with asymmetric contacts (Pd/Bi and Au). (f,g) Output characteristics (f) and photodetector responsivity (g) of few-layer WS_2 photodetector devices with transferred and evaporated electrodes as indicated in the legends.

different types of TMDs. Moreover, by employing different metals as contacts, we show significant changes in transfer characteristics of 1L WSe_2 devices as shown in Figure S11a. All these results indicate that the negligible FL pinning effect can be achieved by diamond-assisted electrode transfer technology. To further quantify the FL pinning factor, we extracted the SBH for three different contact metals for monolayer WSe_2 and plotted them against the metal work function as shown in Figure S11b. The SBH is highly dependent on the work function of the metals. The extracted pinning factor is approximately 0.7 ± 0.2, which is significantly larger than the factor of 0.03 reported for evaporated contacts on WSe_2,[28] indicating a substantial reduction in FL pinning. This result can be attributed to the effective suppression of MIGS by the proposed method in this work. Furthermore, the small deviation from the ideal Schottky limit is likely due to defects present in the exfoliated flakes.[29]

The possibility to pick up and transfer a wide range of metals from the diamond surface to form vdW contacts eliminates the need of *ex situ* lithography and metallization that inevitably expose 2D materials to air. Here, we demonstrate the efficacy of our proposed electrode transfer technology for fabricating devices with air-sensitive materials, such as 1T' WTe_2.[30,31] The diamond transfer technology was used to assemble electrodes on a three-layer 1T' WTe_2 flake in an inert atmosphere followed by passivation with PMMA to make the device suitable for handling in ambient (see Methods and Experiments). As shown in Figure S12b,c, the poly(methyl methacrylate) (PMMA)-coated trilayer WTe_2 device with transferred electrodes exhibits linear $I-V$ characteristics in ambient conditions. In contrast, the reference device fabricated using standard photolithography and PMMA coating shows an insulating behavior under similar atmospheric conditions. This demonstrates the advantage of our device fabrication technology, which can be performed in an oxygen- and moisture-free environment, protecting the materials from oxidation. In contrast, the standard photolithography process cannot completely exclude exposure to atmosphere. Furthermore, the PMMA-coated trilayer WTe_2 device with transferred electrodes experienced minimal degradation (less than 10%) over a 3-day period of measurements (Figure S12d), suggesting its robust stability when utilizing this approach.

This straightforward diamond-assisted technique is not only confined to monolayer TMDs FETs but also holds promise for other few-layer TMDs in diverse applications such as ambipolar transistors, Schottky barrier diodes, and photodetectors. We first

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ACS Nano 2025, 19, 3579–3588

integrated Pd contacts to multilayer WSe_2 on the SiO_2 (285 nm)/Si substrate as depicted in the inset of Figure 6a and clearly demonstrated the symmetric ambipolar carrier transport according to the typical transfer curves (Figure 6a) at room temperature. Figure 6b,c illustrates the linear output curves at room temperature, demonstrating the capability to modulate the conductance of the WSe_2 channel from both negative (hole conduction) and positive (electron conduction) gate bias. For Schottky barrier diode application, we fabricated asymmetric contacts for a few-layer WSe_2 Schottky barrier diode (inset of Figure 6d) through diamond-assisted electrode transfer technology. A pair of asymmetric electrodes, comprising high-work-function metal Au and low-work-function semimetal Bi, was transferred from diamond to a few-layer WSe_2 flake on the SiO_2 (285 nm)/Si substrate. Figure 6d shows the transfer curves of this device under different source-drain voltages. Here, the Pd/Bi electrode was connected to the electrical ground with source-drain voltage applied to Au. The device displayed hole transport at negative gate bias, with the electron transport significantly suppressed due to the large Schottky barrier between Au and WSe_2. The output curves, as shown in Figure 6e, exhibit pronounced rectification behavior depending on the gate bias ranging from −10 to −60 V, with a high rectification ratio of about 10^2 at a low source-drain voltage of $V_{ds} = \pm 0.5$ V, suggesting a significant presence of contact resistance due to the reverse-biased metal−semiconductor junction.[32,33] The detailed band diagram explanation is shown in Figure S13. The Schottky barrier diode with transferred electrodes demonstrates that the FL pinning effect can be minimized with vdW contacts to 2D materials, allowing significant control of the SBH via the choice of metal. As discussed in the transport studies of monolayer TMD devices, evaporated metal electrodes often suffer from an unintentional variation of SBH from electrode to electrode. Here, we demonstrate that the diamond transfer method results in reliably uniform SBH. The measurement details are discussed in the Methods and Experiments section. Three bilayer WS_2 photodetectors were fabricated with evaporated Pd, and one was integrated with transferred Pd. According to Figure 6f, the open-circuit voltage, V_{oc}, is negligible for the device with transferred contacts; however, the evaporated contact devices exhibited varying V_{oc}, ranging from 0.05 to 0.3 V. The significant shift in V_{oc} suggests the uncontrollable asymmetric back-to-back SBH for evaporated electrodes, while the negligible V_{oc} of transferred electrodes indicates the symmetric SBH. To quantify the photodetection efficiency, the photoresponsivity (R) was extracted for each device. The R of the transferred contact device is approximately 5 times larger than that of devices with evaporated contacts, as shown in Figure 6g, indicating the superior photodetection efficiency of the device with transferred contacts.

CONCLUSIONS

In summary, we have demonstrated a reliable universal metal electrode transfer technology for contacting 2D semiconductors without the need for any buffer layers. By employing hydrogenated diamond surfaces, we successfully transferred eight different patterned metals, including high-work-function metals (Pt, Pd, Au, and Ni), low-work-function metals (Cr, Al, and Ti), and a semimetal (Bi). The ease of peeling off from the hydrogenated diamond surface, thanks to its low adhesion nature, preserved their initial geometries without cracks or folding.

The formation of atomically smooth vdW interfaces on 2D semiconductors was directly observed by TEM. The clean and smooth vdW interfaces effectively minimize the FL pinning effect and allow significant control of the SBH through the choice of metal.

We expect that our technology should be compatible with a wide range of other device applications, such as vertical transistors, self-powered photodiodes, and artificial synaptic devices. This proposed technology holds significant promise for wafer-scale device fabrication with the advancement of large-area diamond-based wafers, offering exciting opportunities for large-scale production in the future. Low device-to-device variation by this method also promises high-performance, highly uniform, scalable novel device architectures and devices, such as advanced monolithic integrated circuits and imaging components. Additionally, it provides a promising fabrication strategy for air-sensitive 2D materials, such as 1T' WTe_2, opening avenues for exploring the new physics, such as correlated quantum states or topological states.

METHODS AND EXPERIMENTS

Fabrication of vdW Electrodes/Monolayer TMDs/*h*BN/SiO_2/Si Back-Gate Transistors and Trilayer WTe_2 Two-Terminal Devices. For TMD device fabrication, high-work-function metal (Pd), low-work-function metal (Ti), and semimetal (Bi) were chosen to characterize the device performance. After fabricating the metal electrodes on the hydrogenated surface (Figure 1, steps 1 and 2) by standard photolithography, *h*BN flakes were mechanically exfoliated onto a silicon substrate with 285 nm SiO_2 as the dielectric layer by the blue tape (P/N: 1009R-1.0) technique. Monolayer TMD flakes (WSe_2 and MoS_2) were mechanically exfoliated onto polydimethylsiloxane (PDMS), and their monolayer nature was verified by both optical contrast and photoluminescence spectroscopy. After annealing the *h*BN dielectric in a furnace (500 sccm Ar and 50 sccm O_2 at 500 °C) for 3 h, the targeted monolayer TMDs were transferred on the precleaned *h*BN by the dry transfer technique. Then, the TMD/*h*BN heterostructures were annealed (950 sccm Ar and 50 sccm H_2 at 300 °C) in a furnace for 1 h to remove most of the PDMS residue. Afterward, the selected metal contacts were picked up by using a PC stamp (PC films were coated on thick 3M transparent tapes to minimize folds) as shown in step 3 of Figure 1 and transferred onto the precleaned TMD/*h*BN heterostructures (steps 4, 5, and 6 shown in Figure 1). The *h*BN flakes here were utilized to minimize the hysteresis effect caused by the charge traps in SiO_2, as shown in Figure S14,[34] whereas the transferred contacts have a minimum impact on the formation of hysteresis. In this work, Pt, Pd, Au, Ni, Cr, Ti, and Al were deposited by an e-beam evaporator (~10^{-6} mbar). Bi was thermally evaporated by using a molecular beam epitaxy system (~10^{-9} mbar). Lastly, the PC film was removed by soaking in $CHCl_3$ at 60 °C for 15 min to form the TMD FETs as shown in step 7 of Figure 1 to expose the transferred electrodes for probing or wire bonding.

Regarding the air-sensitive device fabrication, the entire process takes place within a controlled glovebox environment (N_2 ambient). The trilayer WTe_2 flakes were mechanically exfoliated on a SiO_2 substrate by blue tape. Subsequently, a pair of prefabricated electrodes (Au) was picked up from a diamond substrate using a PC stamp and laminated onto the trilayer WTe_2 flake. Finally, a layer of PMMA was spin-coated onto the device and baked at 180 °C for 2 min to protect it from oxidation in the atmosphere after removal from the glovebox, as shown in Figure S12a. For the reference WTe_2 device, we utilized the standard photolithography technology for device fabrication. The spin coating and lift-off process were performed within a controlled glovebox; however, the device was briefly exposed to ambient after developing and before metal deposition.

FIB STEM/TEM and EDS Measurements. To ensure the preparation of high-quality focused ion beam (FIB) lamella from vdW electrodes/TMD/*h*BN, an FEI HELIOS G3 microscope was employed for FIB lamella preparation. FIB lamella preparation followed

https://doi.org/10.1021/acsnano.4c13592
ACS Nano 2025, 19, 3579−3588

the procedure developed for ion beam-sensitive crystals reported in previous work.[35] A JEOL ARM 200F STEM was employed to acquire high-resolution, high-angle annular dark-field (HAADF) and bright-field (BF) STEM images. EDS mapping was performed to confirm the composition of each layer in vdW electrodes/TMD/*h*BN.

Electrical Transport Measurements. The transport behavior of the TMD transistors and Schottky barrier diodes with vdW electrodes was measured in the temperature range of 300−77 K using a TeslatronPT Oxford Cryostat. Two Keithley 2400 source meters were employed to apply the source-drain voltage (V_{ds}) and gate voltage (V_{gs}) and monitor the source-drain current (I_{ds}) and gate leakage current.

Optoelectrical Measurements. The measurements were performed using a confocal microscope system (WITec alpha 300R) with a 50× objective lens (NA = 0.9) in ambient conditions. A 532 nm laser was fiber coupled through a fiber bench with an optical chopper to adjust the power intensity and give the final spot size of 1 μm diameter. The samples were illuminated from the top side on a piezo crystal-controlled scanning stage. One source meter was employed to apply the source-drain voltage and monitor the photocurrent.

Computational Details. We used DFT calculations as implemented in the Vienna ab initio simulation package (VASP) to calculate the exfoliation energy.[36] The Perdew−Burke−Ernzerhof (PBE) form of the generalized gradient approximation (GGA) was used to describe electron exchange and correlation.[37] The kinetic energy cutoff for the plane-wave basis was set to 400 eV. We used a *k*-point mesh with a density of $2\pi \times 0.02$ Å^{-1} for sampling the Brillouin zone. A 20 Å vacuum was added to prevent interactions between periodic images. To obtain the relaxed interface between the metal and the substrate, we used the lattice of the substrate, allowing all atoms to relax except for the bottom two metallic layers. All forces were relaxed to less than 0.01 eV/Å. The DFT-D3 method was used to account for the van der Waals interactions.[26]

ASSOCIATED CONTENT

Data Availability Statement

The main results in this study are available in the arXiv preprint repository.[38] All data are available in the main text or the Supporting Information.

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acsnano.4c13592.

Comparison of different metal transfer technologies, schematic illustration of diamond polishing/hydrogen termination and AFM results for the polished hydrogenated diamond surface, optical images of metal pick-up and transfer from rough unpolished hydrogenagted diamonds, surface conductivity for hydrogenated diamond before and after several picking-up processes, large-scale electrode transfer from hydrogenated diamonds, schematic diagrams for the relaxed structures for different metals/substration combination, cross-section STEM images for Pd/Ti/monolayer MoS_2/*h*BN heterostrucutres, output curves for monolayer TMD transistors with evaporated and transferred electrodes at room temperature, transport characterizations of another set of transferred electrodes/monolayer TMDs FETs, transport characterizations for 10 CVD-grown MoS_2 FETs, Arrhenius plots extracted from transfer curves of three TMDs FETs, transfer curves for 1L WSe_2 FETs with transferred Au/Ag and Au contacts and experimentally determined Schottky barrier heights (SBH) for different transferred metals on 1L WSe_2 plotted as a function of the metal work function, transport characterizations for few-layer air-sensitive TMD (trilayer 1T' WTe_2), band diagram of WSe_2 contacted with asymmetric contacts, and transfer curves for 1L TMD (MoS_2 and WSe_2) FETs with/without *h*BN (PDF)

Metal pick-up from SiO_2 (MP4)

Metal pick-up from diamond (MP4)

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https://doi.org/10.1021/acsnano.4c13592
ACS Nano 2025, 19, 3579−3588

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†K.X., D.M., and Y.Y. contributed equally to this work. K.X., D.-C.Q., and M.S.F. conceived this research. K.X. designed the experiments. K.X., D.M., and A.S. led the sample fabrication with the assistance of T.-H.-Y.V. and Y.-H.C.. K.X. and W.Z. led the electrical characterization. A.B. and DC. performed the cross-section HRTEM and EDS measurements. M.T.E. helped with the Bi growth. J.H. provided the TMD (WSe_2, MoS_2, and WTe_2) crystals. K.W. and T.T. provided the *h*BN crystals. K.X., J.L., and Q.O. led the photodetector measurements. Y.Y. led the DFT calculation. The manuscript was written through contributions of all authors. All authors have given approval to the final version of this manuscript.

Notes

The authors declare no competing financial interest.

ACKNOWLEDGMENTS

K.X., T.-H.-Y.V., M.T.E., and M.S.F. acknowledge support from ARC grant DP200101345. D.M., W.Z., Y.-H.C., Y.Y., N.V.M., and M.S.F. acknowledge support from the ARC Centre of Excellence in Future Low-Energy Electronics Technologies (FLEET; CE170100039). Y.Y. and N.V.M. acknowledge computational support from the Australian National Computing Infrastructure (NCI), Pawsey Supercomputing Centre. M.T.E. acknowledges support from ARC grant FT220100290. D.-C.Q. acknowledges support of the Australian Research Council (Grant No. DP230101904). D.-C.Q. acknowledges continued support from the Queensland University of Technology (QUT) through the Centre for Materials Science. A.S. acknowledges support of the Australian Research Council (Grant No. LP190100528). K.W. and T.T. acknowledge support from the JSPS KAKENHI (Grant Numbers 21H05233 and 23H02052) and World Premier International Research Center Initiative (WPI), MEXT, Japan. Q.O. acknowledges support from the Science and Technology Development Fund, Macau SAR (No. 0065/2023/AFJ, No. 0116/2022/A3, and No. 0009/2022/AGJ), the National Natural Science Foundation of China (52402166), and the Australian Research Council (DE220100154). The microscopy was enabled by the Electron Microscopy Centre at the University of Wollongong and used the FEI Helios G3 CX funded by the ARC LIEF grant (No. LE160100063) and the JEOL JEM-ARM200F funded by the ARC LIEF grant (No. LE120100104). This work was performed in part at the Melbourne Centre for Nanofabrication (MCN) in the Victorian Node of the Australian National Fabrication Facility (ANFF) with M. E. ANFF-VIC Technology Fellowship.

REFERENCES

(1) Liu, Y.; Duan, X.; Shin, H.-J.; Park, S.; Huang, Y.; Duan, X. Promises and Prospects of Two-Dimensional Transistors. *Nature* **2021**, *591* (7848), 43−53.
(2) Tan, T.; Jiang, X.; Wang, C.; Yao, B.; Zhang, H. 2D Material Optoelectronics for Information Functional Device Applications: Status and Challenges. *Adv. Sci.* **2020**, *7* (11), No. 2000058.
(3) Yang, H.; Valenzuela, S. O.; Chshiev, M.; Couet, S.; Dieny, B.; Dlubak, B.; Fert, A.; Garello, K.; Jamet, M.; Jeong, D.-E.; Lee, K.; Lee, T.; Martin, M.-B.; Kar, G. S.; Sénéor, P.; Shin, H.-J.; Roche, S. Two-Dimensional Materials Prospects for Non-VolatileSpintronic Memories. *Nature* **2022**, *606* (7915), 663−673.
(4) Franklin, A. D. Nanomaterials in Transistors: From High-Performance to Thin-Film Applications. *Science* **2015**, *349* (6249), No. aab2750.
(5) Allain, A.; Kang, J.; Banerjee, K.; Kis, A. Electrical Contacts to Two-Dimensional Semiconductors. *Nat. Mater.* **2015**, *14* (12), 1195−1205.
(6) Schulman, D. S.; Arnold, A. J.; Das, S. Contact Engineering for 2D Materials and Devices. *Chem. Soc. Rev.* **2018**, *47* (9), 3037−3058.
(7) Kim, C.; Moon, I.; Lee, D.; Choi, M. S.; Ahmed, F.; Nam, S.; Cho, Y.; Shin, H.-J.; Park, S.; Yoo, W. J. Fermi Level Pinning at Electrical Metal Contacts of Monolayer Molybdenum Dichalcogenides. *ACS Nano* **2017**, *11* (2), 1588−1596.
(8) Smyth, C. M.; Addou, R.; Hinkle, C. L.; Wallace, R. M. Origins of Fermi-Level Pinning between Molybdenum Dichalcogenides ($MoSe_2$, $MoTe_2$) and Bulk Metal Contacts: Interface Chemistry and Band Alignment. *J. Phys. Chem. C* **2019**, *123* (39), 23919−23930.
(9) Wang, Y.; Kim, J. C.; Wu, R. J.; Martinez, J.; Song, X.; Yang, J.; Zhao, F.; Mkhoyan, A.; Jeong, H. Y.; Chhowalla, M. Van Der Waals Contacts between Three-Dimensional Metals and Two-Dimensional Semiconductors. *Nature* **2019**, *568* (7750), 70−74.
(10) Wang, Y.; Kim, J. C.; Li, Y.; Ma, K. Y.; Hong, S.; Kim, M.; Shin, H. S.; Jeong, H. Y.; Chhowalla, M. P-Type Electrical Contacts for 2D Transition-Metal Dichalcogenides. *Nature* **2022**, *610* (7930), 61−66.
(11) Shen, P.-C.; Su, C.; Lin, Y.; Chou, A.-S.; Cheng, C.-C.; Park, J.-H.; Chiu, M.-H.; Lu, A.-Y.; Tang, H.-L.; Tavakoli, M. M.; Pitner, G.; Ji, X.; Cai, Z.; Mao, N.; Wang, J.; Tung, V.; Li, J.; Bokor, J.; Zettl, A.; Wu, C.-I.; et al. Ultralow Contact Resistance between Semimetal and Monolayer Semiconductors. *Nature* **2021**, *593* (7858), 211−217.
(12) Li, W.; Gong, X.; Yu, Z.; Ma, L.; Sun, W.; Gao, S.; Köroğlu, Ç.; Wang, W.; Liu, L.; Li, T.; Ning, H.; Fan, D.; Xu, Y.; Tu, X.; Xu, T.; Sun, L.; Wang, W.; Lu, J.; Ni, Z.; Li, J.; et al. Approaching the Quantum Limit in Two-Dimensional Semiconductor Contacts. *Nature* **2023**, *613* (7943), 274−279.
(13) Wen, X.; Lei, W.; Li, X.; Di, B.; Zhou, Y.; Zhang, J.; Zhang, Y.; Li, L.; Chang, H.; Zhang, W. $ZrTe_2$ Compound Dirac Semimetal Contacts for High-Performance MoS_2 Transistors. *Nano Lett.* **2023**, *23* (18), 8419−8425.
(14) Santosh, K. C.; Longo, R. C.; Addou, R.; Wallace, R. M.; Cho, K. Electronic Properties of MoS_2/MoO_x Interfaces: Implications in

Tunnel Field Effect Transistors and Hole Contacts. *Sci. Rep.* **2016**, *6* (1), 33562.
(15) Chen, Y.-H.; Xing, K.; Liu, S.; Holtzman, L. N.; Creedon, D. L.; McCallum, J. C.; Watanabe, K.; Taniguchi, T.; Barmak, K.; Hone, J.; Hamilton, A. R.; Chen, S.-Y.; Fuhrer, M. S. P-Type Ohmic Contact to Monolayer WSe_2 Field-Effect Transistors Using High-Electron Affinity Amorphous MoO_3. *ACS Appl. Electron. Mater.* **2022**, *4* (11), 5379−5386.
(16) Liu, Y.; Guo, J.; Zhu, E.; Liao, L.; Lee, S.-J.; Ding, M.; Shakir, I.; Gambin, V.; Huang, Y.; Duan, X. Approaching the Schottky−Mott Limit in Van Der Waals Metal−Semiconductor Junctions. *Nature* **2018**, *557* (7707), 696−700.
(17) Liu, G.; Tian, Z.; Yang, Z.; Xue, Z.; Zhang, M.; Hu, X.; Wang, Y.; Yang, Y.; Chu, P. K.; Mei, Y.; Liao, L.; Hu, W.; Di, Z. Graphene-Assisted Metal Transfer Printing for Wafer-Scale Integration of Metal Electrodes and Two-Dimensional Materials. *Nat. Electron.* **2022**, *5* (5), 275−280.
(18) Zhang, X.; Huang, C.; Li, Z.; Fu, J.; Tian, J.; Ouyang, Z.; Yang, Y.; Shao, X.; Han, Y.; Qiao, Z.; Zeng, H. Reliable Wafer-Scale Integration of Two-Dimensional Materials and Metal Electrodes with Van Der Waals Contacts. *Nat. Commun.* **2024**, *15* (1), 4619.
(19) Kwon, G.; Choi, Y.-H.; Lee, H.; Kim, H.-S.; Jeong, J.; Jeong, K.; Baik, M.; Kwon, H.; Ahn, J.; Lee, E.; Cho, M.-H. Interaction- and Defect-Free Van Der Waals Contacts between Metals and Two-Dimensional Semiconductors. *Nat. Electron.* **2022**, *5* (4), 241−247.
(20) Kong, L.; Wu, R.; Chen, Y.; Huangfu, Y.; Liu, L.; Li, W.; Lu, D.; Tao, Q.; Song, W.; Li, W.; Lu, Z.; Liu, X.; Li, Y.; Li, Z.; Tong, W.; Ding, S.; Liu, S.; Ma, L.; Ren, L.; Wang, Y.; et al. Wafer-Scale and Universal Van Der Waals Metal Semiconductor Contact. *Nat. Commun.* **2023**, *14* (1), 1014.
(21) Yi, K.; Wu, Y.; An, L.; Deng, Y.; Duan, R.; Yang, J.; Zhu, C.; Gao, W.; Liu, Z. Van Der Waals Encapsulation by Ultrathin Oxide for Air-Sensitive 2D Materials. *Adv. Mater.* **2024**, *36* (33), No. 2403494.
(22) Lee, H. Y.; Wang, Z.; Chen, G.; Holtzman, L. N.; Yan, X.; Amontree, J.; Zangiabadi, A.; Watanabe, K.; Taniguchi, T.; Barmak, K.; Kim, P.; Hone, J. C. In Situ via Contact to hBN-Encapsulated Air-Sensitive Atomically Thin Semiconductors. *ACS Nano* **2024**, *18* (26), 17111−17118.
(23) Riedel, M.; Ristein, J.; Ley, L. Recovery of Surface Conductivity of H-Terminated Diamond after Thermal Annealing in Vacuum. *Phys. Rev. B* **2004**, *69* (12), No. 125338.
(24) Xing, K.; Zhang, S.; Tsai, A.; Xiao, Y.; Creedon, D. L.; Yianni, S. A.; McCallum, J. C.; Pakes, C. I.; Qi, D.-C. High-Electron-Affinity Oxides V_2O_5 Enhances Surface Transfer Doping on Hydrogen-Terminated Diamond. *Diam. Relat. Mater.* **2020**, *108*, No. 107865.
(25) Yang, X.; Li, J.; Song, R.; Zhao, B.; Tang, J.; Kong, L.; Huang, H.; Zhang, Z.; Liao, L.; Liu, Y.; Duan, X.; Duan, X. Highly Reproducible Van Der Waals Integration of Two-Dimensional Electronics on the Wafer Scale. *Nat. Nanotechnol.* **2023**, *18* (5), 471−478.
(26) Grimme, S.; Antony, J.; Ehrlich, S.; Krieg, H. A Consistent and Accurate Ab Initio Parametrization of Density Functional Dispersion Correction (DFT-D) for the 94 Elements H-Pu. *J. Chem. Phys.* **2010**, *132* (15), 154104.
(27) Fonseca, A. F.; Liang, T.; Zhang, D.; Choudhary, K.; Phillpot, S. R.; Sinnott, S. B. Graphene-Titanium Interfaces from Molecular Dynamics Simulations. *ACS Appl. Mater. Interfaces* **2017**, *9* (38), 33288−33297.
(28) Jang, J.; Ra, H.-S.; Ahn, J.; Kim, T. W.; Song, S. H.; Park, S.; Taniguch, T.; Watanabe, K.; Lee, K.; Hwang, D. K. Fermi-Level Pinning-Free WSe_2 Transistors via 2D Van der Waals Metal Contacts and Their Circuits. *Adv. Mater.* **2022**, *34* (19), No. 2109899.
(29) Chen, Y.-H.; Cheng, C.-Y.; Chen, S.-Y.; Rodriguez, J. S. D.; Liao, H.-T.; Watanabe, K.; Taniguchi, T.; Chen, C.-W.; Sankar, R.; Chou, F.-C.; Chiu, H.-C.; Wang, W.-H. Oxidized-Monolayer Tunneling Barrier for Strong Fermi-Level Depinning in Layered InSe Transistors. *NPJ 2D Mater. Appl.* **2019**, *3* (1), 49.
(30) Ye, F.; Lee, J.; Hu, J.; Mao, Z.; Wei, J.; Feng, P. X.-L. Environmental Instability and Degradation of Single- and Few-Layer WTe_2 Nanosheets in Ambient Conditions. *Small* **2016**, *12* (42), 5802−5808.
(31) Hou, F.; Zhang, D.; Sharma, P.; Singh, S.; Wu, T.; Seidel, J. Oxidation Kinetics of WTe_2 Surfaces in Different Environments. *ACS Appl. Electron. Mater.* **2020**, *2* (7), 2196−2202.
(32) Kim, J.; Venkatesan, A.; Phan, N. A. N.; Kim, Y.; Kim, H.; Whang, D.; Kim, G.-H. Schottky Diode with Asymmetric Metal Contacts on WS_2. *Adv. Electron. Mater.* **2022**, *8* (3), No. 2100941.
(33) Zhou, C.; Zhang, S.; Lv, Z.; Ma, Z.; Yu, C.; Feng, Z.; Chan, M. Self-Driven WSe_2 Photodetectors Enabled with Asymmetrical Van Der Waals Contact Interfaces. *NPJ 2D Mater. Appl.* **2020**, *4* (1), 46.
(34) Illarionov, Y. Y.; Rzepa, G.; Waltl, M.; Knobloch, T.; Grill, A.; Furchi, M. M.; Mueller, T.; Grasser, T. The Role of Charging Trapping in MoS_2/SiO_2 and MoS_2/hBN Field-Effect Transistors. *2D Mater.* **2016**, *3* (3), No. 035004.
(35) Bake, A.; Zhao, W.; Mitchell, D.; Wang, X.; Nancarrow, M.; Cortie, D. Lamellae Preparation for Atomic-Resolution STEM Imaging from Ion-Beam-Sensitive Topological Insulator Crystals. *J. Vac. Sci. Technol. A* **2022**, *40* (3), No. 033203.
(36) Kresse, G.; Furthmüller, J. Efficiency of Ab-Initio Total Energy Calculations for Metals and Semiconductors Using a Plane-Wave Basis. *Set. Comp. Nater. Sci.* **1996**, *6* (1), 15−50.
(37) Perdew, J. P.; Burke, K.; Ernzerhof, M. Generalized Gradient Approximation Made Simple. *Phys. Rev. Lett.* **1996**, *77* (18), 3865−3868.
(38) Xing, K.; McEwen, D.; Zhao, W.; Bake, A.; Cortie, D.; Liu, J.; Vu, T.-H.-Y.; Hone, J.; Stacey, A.; Edmonds, M.; Watanabe, K.; Taniguchi, T.; Ou, Q.; Qi, D.-C.; Fuhrer, M. S. Pick-and-Place Transfer of Arbitrary-Metal Electrodes for Van Der Waals Device Fabrication. 2024. *arXiv*. http://arxiv.org/abs/2405.12830.

https://doi.org/10.1021/acsnano.4c13592
ACS Nano 2025, 19, 3579−3588